

8

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1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DRAWING

REV

02

ZONE

ECN

248015

DESCRIPTION OF CHANGE

ENGINEERING RELEASED

CK APPD

ENG APPD

DATE

12/05/02

DATE

?

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PAGE

43

COMPONENT LOCATIONS (2 OF 2)

SCHEM,MLB,PB15

Fri Jan 23 20:30:40 2004

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
SSCG	NO_SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
USB_MODEM	SOFT_MODEM
GPU_PWRMSR	INT_TMDS
GPU_SS	
VGA_BUFFER_RES	
EXT_TMDS	

DIMENSIONS ARE IN MILLIMETERS

XX : _____

X.XX : _____

X.XXX : _____

ANGLES : _____

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER	/	DESIGN CK	/
ENG APPD	/	MFG APPD	/
QA APPD	/	DESIGNER	/
RELEASE	/	SCALE	NONE
MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D

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TITLE

SCHEM,MLB,PB15"

DRAWING NUMBER	051-6338	REV.	C
SHT		1	OF 40

8

7

6

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2

1

PART#

QTY

DESCRIPTION

REFERENCE DESIGNATOR(S)

BOM OPTION

051-6338

1

SCHEM,MLB,PB15

SCH1

820-1441

1

PCBF,MLB,PB15

PCB1

065-3951

1

CMNPRTS,MLB,PB15

DMS1

DMS630-4285&DMS630-4721

065-3952

1

SELPRTS,MLB,PB15,BTR

DMS2

DMS630-4285

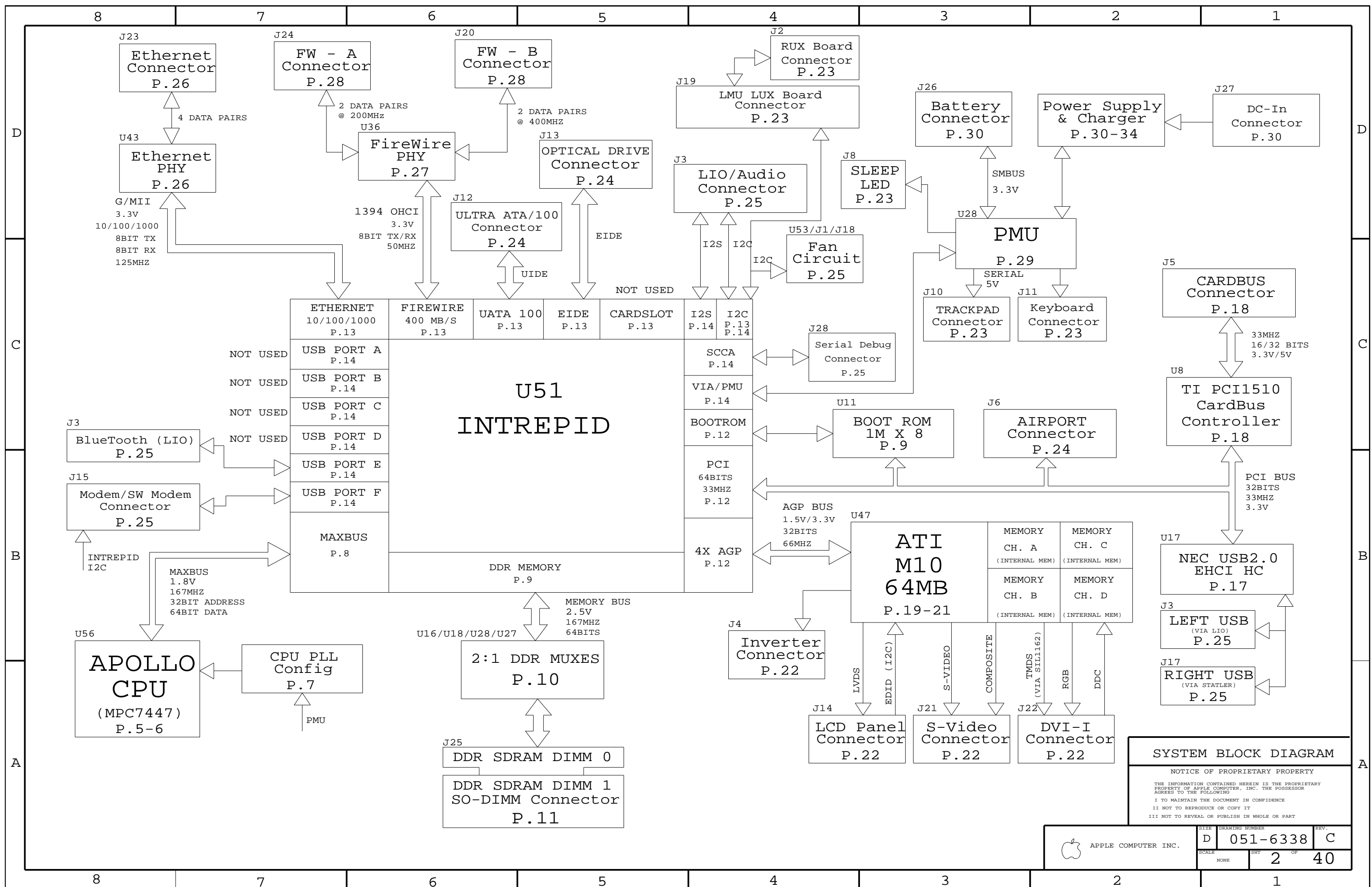
065-4479

1

SELPRTS,MLB,PB15,BST

DMS3

DMS630-4721



POWER SYSTEM ARCHITECTURE

The diagram illustrates the power system architecture, showing the flow of power from the AC adapter and battery through various regulators and sequencers to the system components.

Power Sources:

- AC ADAPTER IN (PG 30):** Provides +24V_PBUS and +3V_PMU LDO (PG 31).
- BACKUP BATTERY (PG 31):** Provides +BATT and +3V_PMU LDO (PG 31).
- 3S 2P 18650 CELLS:** Provides +BATT and BATTERY VOLTAGE FEED-IN PATH (PG 30).

Regulators and Sequencers:

- INRUSH LIMITER (PG 30):** Limits inrush current from the AC adapter.
- BUCK REGULATOR (LTC1625) (PG 31):** Converts +24V_PBUS to +5V_MAIN.
- MAIN 3V/5V DC/DC (LTC3707) (PG 32 STBYMD):** Converts +5V_MAIN to +3V_5V_OK and +3V_MAIN.
- DC/DC (LTC3411) (PG 34):** Converts +3V_MAIN to +1.8V_MAIN (MAXBUS).
- EXT VCC DC/DC (LTC1778) (PG 20):** Converts +5V_MAIN to GPU_VCORE +1.2V.
- DC/DC (MAX1717) (PG 33):** Converts +5V_MAIN to CPU_VCORE (+1.385V).
- MAXBUS SEQUENCING:** Controls the power-up and power-down sequence of the system.

Timing Diagram:

The timing diagram shows the power-up and power-down sequence. The signals are: SHUT-DOWN, RUN, SLEEP, RUN, SHUT-DOWN. The signals are: SLEEP, SLEEP_L_LS5, DCDC_EN, DCDC_EN_L, +5V_MAIN, +5V_SLEEP, +3V_MAIN, +3V_SLEEP, 3V_5V_OK, +2_5V_MAIN, +2_5V_SLEEP, +1_5V_MAIN, +1_5V_SLEEP, 1_5V_2_5V_OK (MAX1715 OUTPUT), 1_5V_2_5V_OK (AT LTC1778 RUN/SS), GPU_VCORE (D3HOT), GPU_VCORE (D3COLD).

POWER BLOCK DIAGRAM

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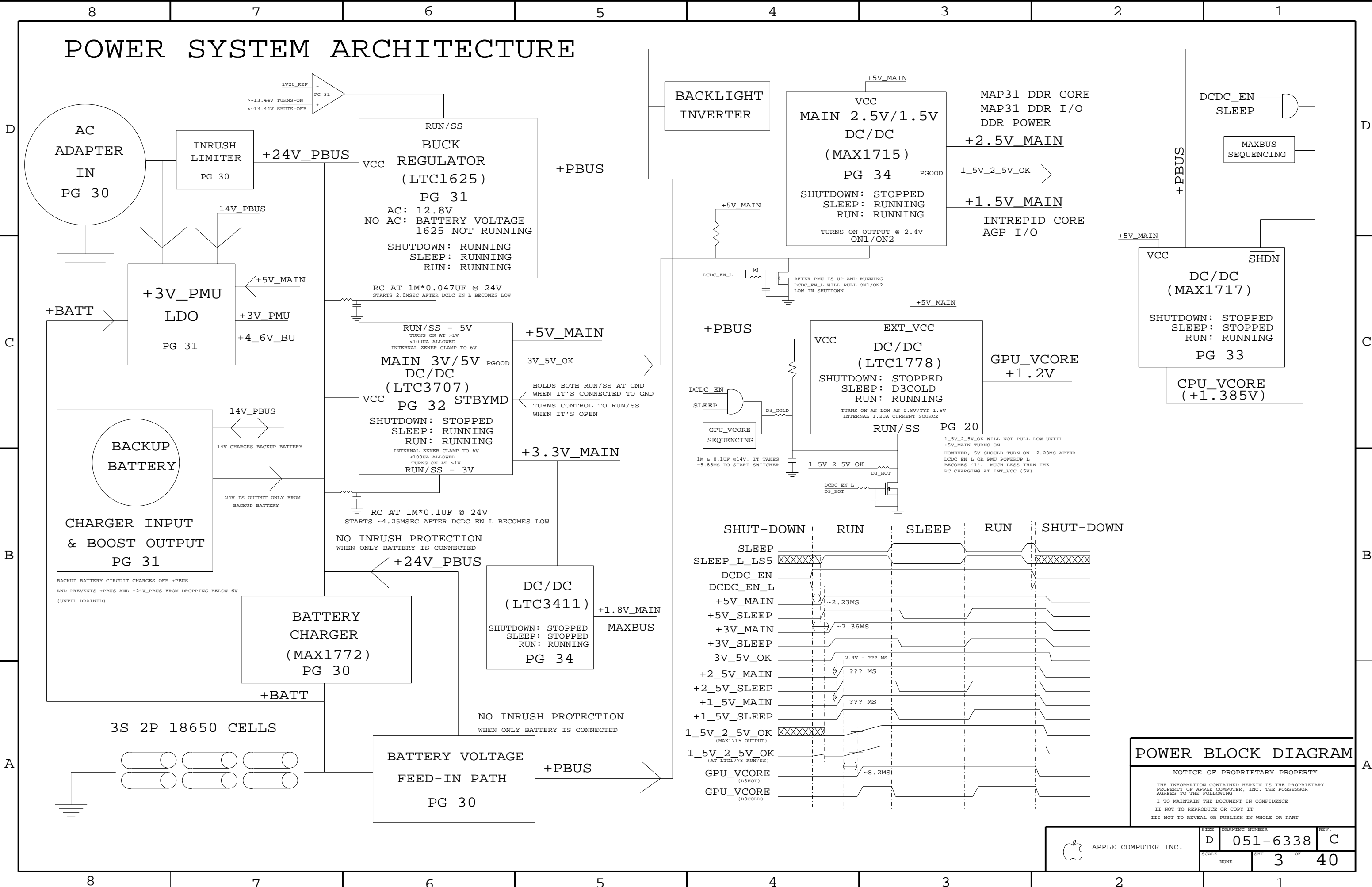
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SIZE DRAWING NUMBER REV.
D 051-6338 C

SCALE SHT OF
NONE 3 40



POWER SYSTEM ARCHITECTURE

The diagram illustrates the power system architecture, showing the flow of power from the AC adapter and battery through various regulators and sequencers to the system components.

Power Sources:

- AC ADAPTER IN (PG 30):** Provides +24V_PBUS and +3V_PMU LDO (PG 31).
- BACKUP BATTERY (PG 31):** Provides +BATT and +3V_PMU LDO (PG 31).
- 3S 2P 18650 CELLS:** Provides +BATT and +24V_PBUS.

Regulators and Sequencers:

- INRUSH LIMITER (PG 30):** Protects the AC adapter input.
- BUCK REGULATOR (LTC1625) (PG 31):** Converts +24V_PBUS to +5V_MAIN.
- MAIN 3V/5V DC/DC (LTC3707) (PG 32 STBYMD):** Converts +5V_MAIN to +3V_5V_OK and +3V_MAIN.
- DC/DC (LTC3411) (PG 34):** Converts +3V_MAIN to +1.8V_MAIN (MAXBUS).
- EXT VCC DC/DC (LTC1778) (PG 20):** Converts +5V_MAIN to GPU_VCORE (+1.2V).
- DC/DC (MAX1717) (PG 33):** Converts +5V_MAIN to CPU_VCORE (+1.385V).
- MAX31715 DC/DC (PG 34):** Converts +5V_MAIN to +2.5V_MAIN and +1.5V_MAIN.
- MAX1772 BATTERY CHARGER (PG 30):** Charges the backup battery.

Timing Diagram:

The timing diagram shows the sequence of events during power-up and shutdown. Key signals include SLEEP, DCDC_EN, DCDC_EN_L, +5V_MAIN, +5V_SLEEP, +3V_MAIN, +3V_SLEEP, 3V_5V_OK, +2_5V_MAIN, +2_5V_SLEEP, +1_5V_MAIN, +1_5V_SLEEP, 1_5V_2_5V_OK (MAX1715 OUTPUT), 1_5V_2_5V_OK (AT LTC1778 RUN/SS), GPU_VCORE (D3HOT), and GPU_VCORE (D3COLD).

POWER BLOCK DIAGRAM

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SCALE: NONE SHT: 3 OF 40

POWER SYSTEM ARCHITECTURE

The diagram illustrates the power system architecture, showing the flow of power from the AC adapter and battery through various regulators and sequencers to the system components.

Power Sources:

- AC ADAPTER IN (PG 30):** Provides +24V_PBUS and +3V_PMU LDO (PG 31).
- BACKUP BATTERY (PG 31):** Provides +BATT and +3V_PMU LDO (PG 31).
- 3S 2P 18650 CELLS (PG 30):** Provides +BATT and BATTERY VOLTAGE FEED-IN PATH (PG 30).

Regulators and Sequencers:

- INRUSH LIMITER (PG 30):** Protects the system from inrush current.
- BUCK REGULATOR (LTC1625) (PG 31):** Converts +24V_PBUS to +5V_MAIN.
- MAIN 3V/5V DC/DC (LTC3707) (PG 32 STBYMD):** Converts +5V_MAIN to +3V_5V_OK and +3V_MAIN.
- DC/DC (LTC3411) (PG 34):** Converts +3V_MAIN to +1.8V_MAIN (MAXBUS).
- EXT VCC DC/DC (LTC1778) (PG 20):** Converts +5V_MAIN to GPU_VCORE +1.2V.
- DC/DC (MAX1717) (PG 33):** Converts +5V_MAIN to CPU_VCORE (+1.385V).
- DC/DC (MAX1715) (PG 34):** Converts +5V_MAIN to +2.5V_MAIN and +1.5V_MAIN.
- BATTERY CHARGER (MAX1772) (PG 30):** Charges the backup battery.

Timing Diagram:

The timing diagram shows the sequence of events during power-up and shutdown. The signals are:

- SLEEP
- SLEEP_L_LS5
- DCDC_EN
- DCDC_EN_L
- +5V_MAIN
- +5V_SLEEP
- +3V_MAIN
- +3V_SLEEP
- 3V_5V_OK
- +2_5V_MAIN
- +2_5V_SLEEP
- +1_5V_MAIN
- +1_5V_SLEEP
- 1_5V_2_5V_OK (MAX1715 OUTPUT)
- 1_5V_2_5V_OK (AT LTC1778 RUN/SS)
- GPU_VCORE (D3HOT)
- GPU_VCORE (D3COLD)

POWER BLOCK DIAGRAM

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SCALE: NONE SHT 3 OF 40

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA				SIGNAL (1/2 OZ + COPPER PLATING)			
1				SIGNAL (1/2 OZ)			
2	PREPREG (3 MIL)			GROUND (1/2 OZ)			
3	PREPREG (3 MIL)			CUT POWER PLANE (1 OZ)			
4	CORE (3 MIL)			CUT POWER PLANE (1 OZ)			
5	PREPREG (5 MIL)			SIGNAL (1/2 OZ)			
6	CORE (5 MIL)			GROUND (1/2 OZ)			
7	PREPREG (5 MIL)			SIGNAL (1/2 OZ + COPPER PLATING)			
8	CORE (3 MIL)						
9	PREPREG (3 MIL)						
10	PREPREG (3 MIL)						

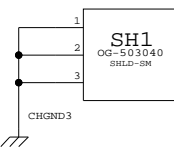
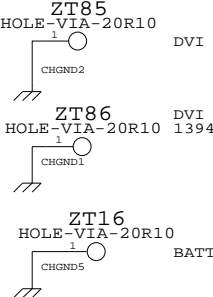
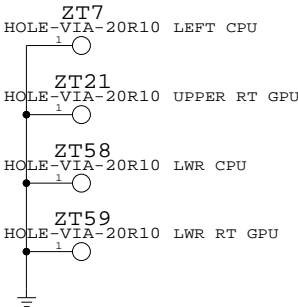
BOARD HOLES

CHASSIS MOUNTS

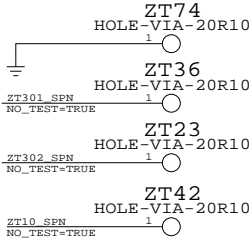
ASICS HEATSINK MOUNTS

I/O AREA

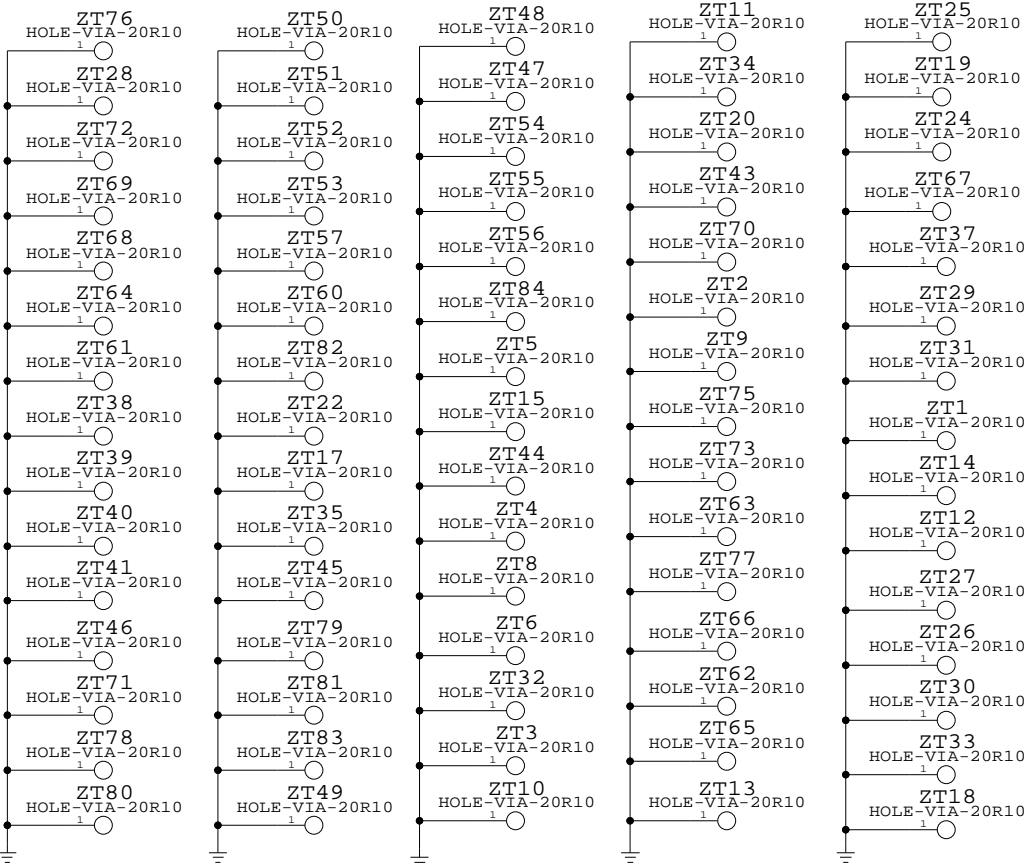
INVERTER



MECH. HOLES



GROUND VIAS



BOARD INFORMATION

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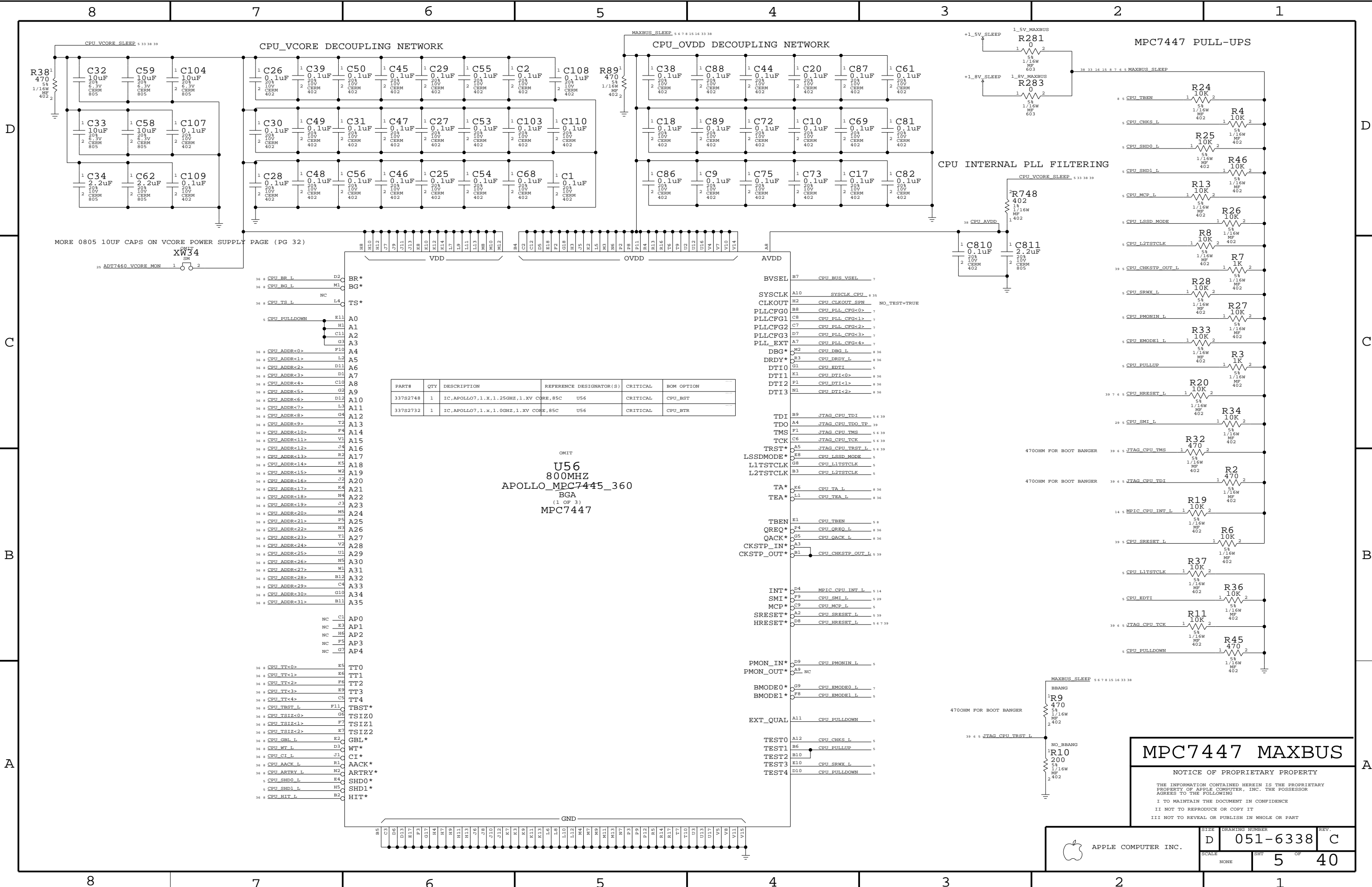
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SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE	SHT	OF
NONE	4	40



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2748	1	IC, APOLLO7, 1.1 X, 1.25GHZ, 1.XV CORE, 85C	U56	CRITICAL	CPU_BST
337S2732	1	IC, APOLLO7, 1.1 X, 1.0GHZ, 1.XV CORE, 85C	U56	CRITICAL	CPU_BTR

U56
800MHZ
APOLLO_MPC7445_360
BGA
(1 OF 3)
MPC7447

MPC7447 MAXBUS

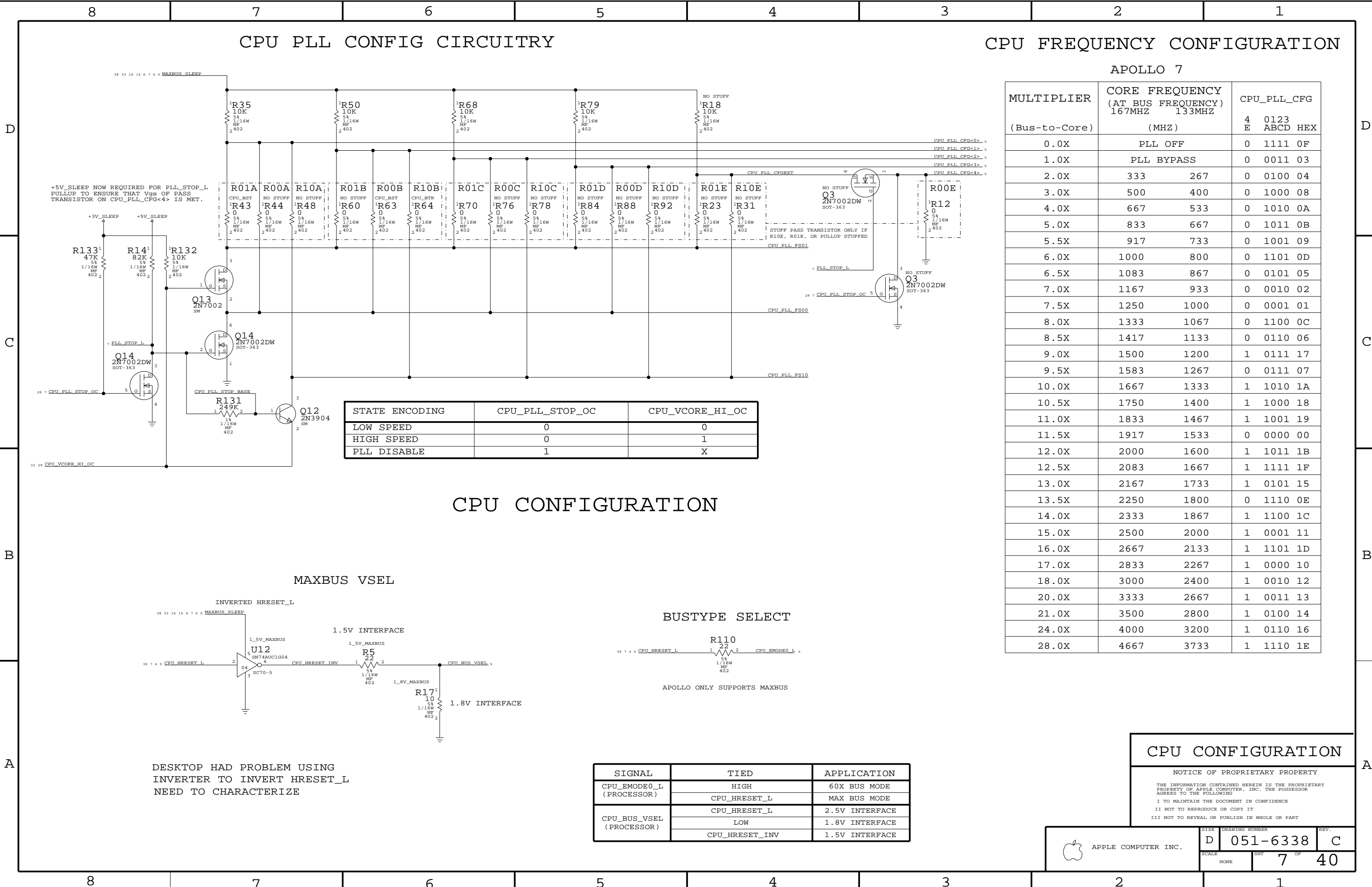
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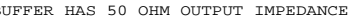
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8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



D_0	D10	CPU DATA<0>	5	36
D_1	G12	CPU DATA<1>	5	36
D_2	E11	CPU DATA<2>	5	36
D_3	H11	CPU DATA<3>	5	36
D_4	B9	CPU DATA<4>	5	36
D_5	N8	CPU DATA<5>	5	36
D_6	H8	CPU DATA<6>	5	36
D_7	A8	CPU DATA<7>	5	36
D_8	E12	CPU DATA<8>	5	36
D_9	D11	CPU DATA<9>	5	36
D_10	B10	CPU DATA<10>	5	36
D_11	J13	CPU DATA<11>	5	36
D_12	A10	CPU DATA<12>	5	36
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D_23	G15	CPU DATA<23>	5	36
D_24	B13	CPU DATA<24>	5	36
D_25	H15	CPU DATA<25>	5	36
D_26	D14	CPU DATA<26>	5	36
D_27	B14	CPU DATA<27>	5	36
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D_30	E15	CPU DATA<30>	5	36
D_31	J16	CPU DATA<31>	5	36
D_32	D15	CPU DATA<32>	5	36
D_33	A14	CPU DATA<33>	5	36
D_34	A13	CPU DATA<34>	5	36
D_35	D16	CPU DATA<35>	5	36
D_36	E16	CPU DATA<36>	5	36
D_37	G17	CPU DATA<37>	5	36
D_38	B15	CPU DATA<38>	5	36
D_39	H17	CPU DATA<39>	5	36
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D_42	E17	CPU DATA<42>	5	36
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D_44	J18	CPU DATA<44>	5	36
D_45	H18	CPU DATA<45>	5	36
D_46	D17	CPU DATA<46>	5	36
D_47	G18	CPU DATA<47>	5	36
D_48	A17	CPU DATA<48>	5	36
D_49	B17	CPU DATA<49>	5	36
D_50	E18	CPU DATA<50>	5	36
D_51	B18	CPU DATA<51>	5	36
D_52	D18	CPU DATA<52>	5	36
D_53	A18	CPU DATA<53>	5	36
D_54	A19	CPU DATA<54>	5	36
D_55	H19	CPU DATA<55>	5	36
D_56	B19	CPU DATA<56>	5	36
D_57	J19	CPU DATA<57>	5	36
D_58	A20	CPU DATA<58>	5	36
D_59	D19	CPU DATA<59>	5	36
D_60	E19	CPU DATA<60>	5	36
D_61	G19	CPU DATA<61>	5	36
D_62	B20	CPU DATA<62>	5	36
D_63	G20	CPU DATA<63>	5	36
DBG	A30	CPU DBG L	5	36
DRDY	C28	CPU DRDY L	5	36
DTI_0	K25	CPU DTI<0>	5	36
DTI_1	O29	CPU DTI<1>	5	36
DTI_2	B30	CPU DTI<2>	5	36
TA	E27	CPU TA L	5	36
TEA	E28	CPU TEA L	5	36



C



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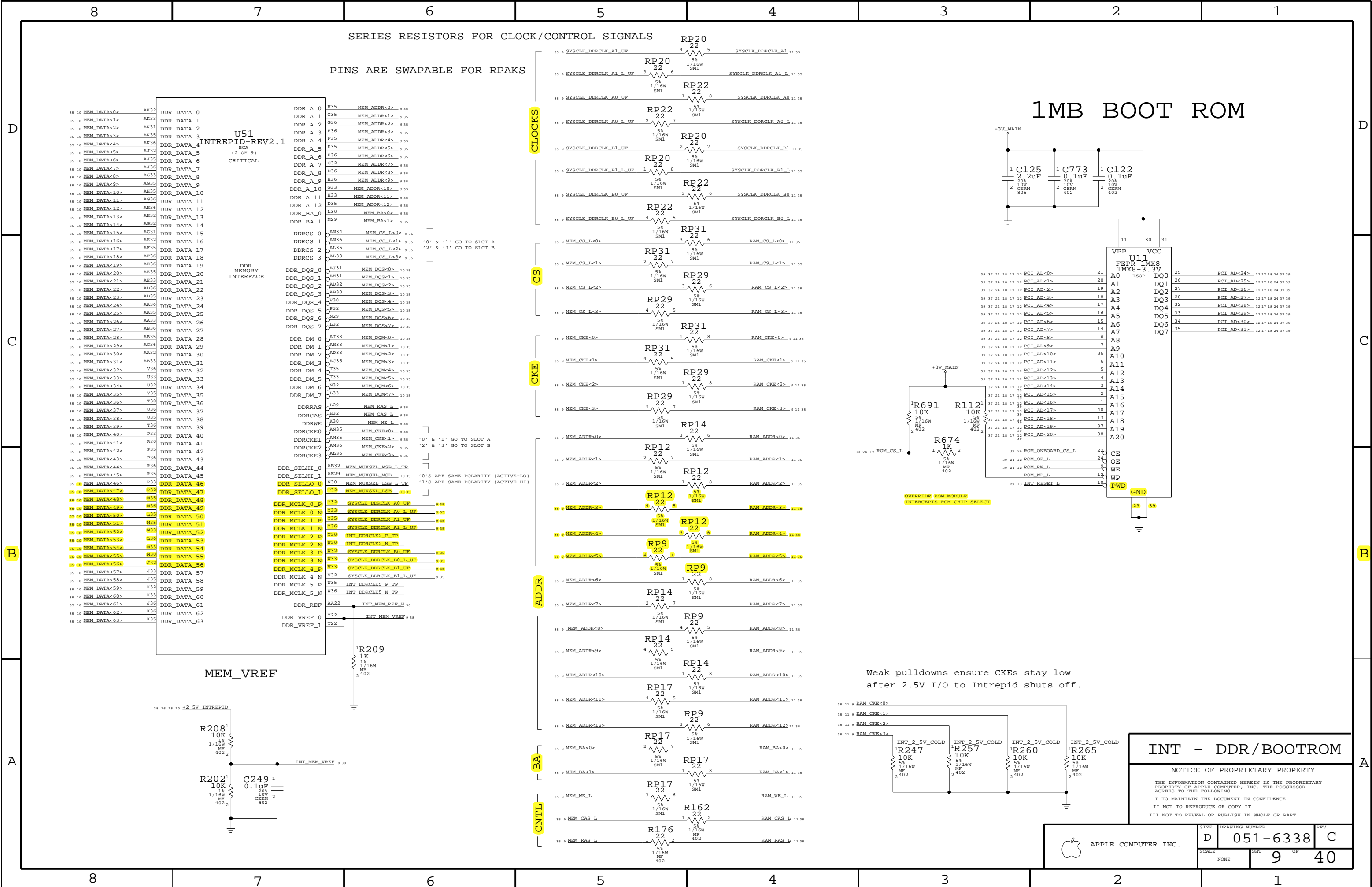
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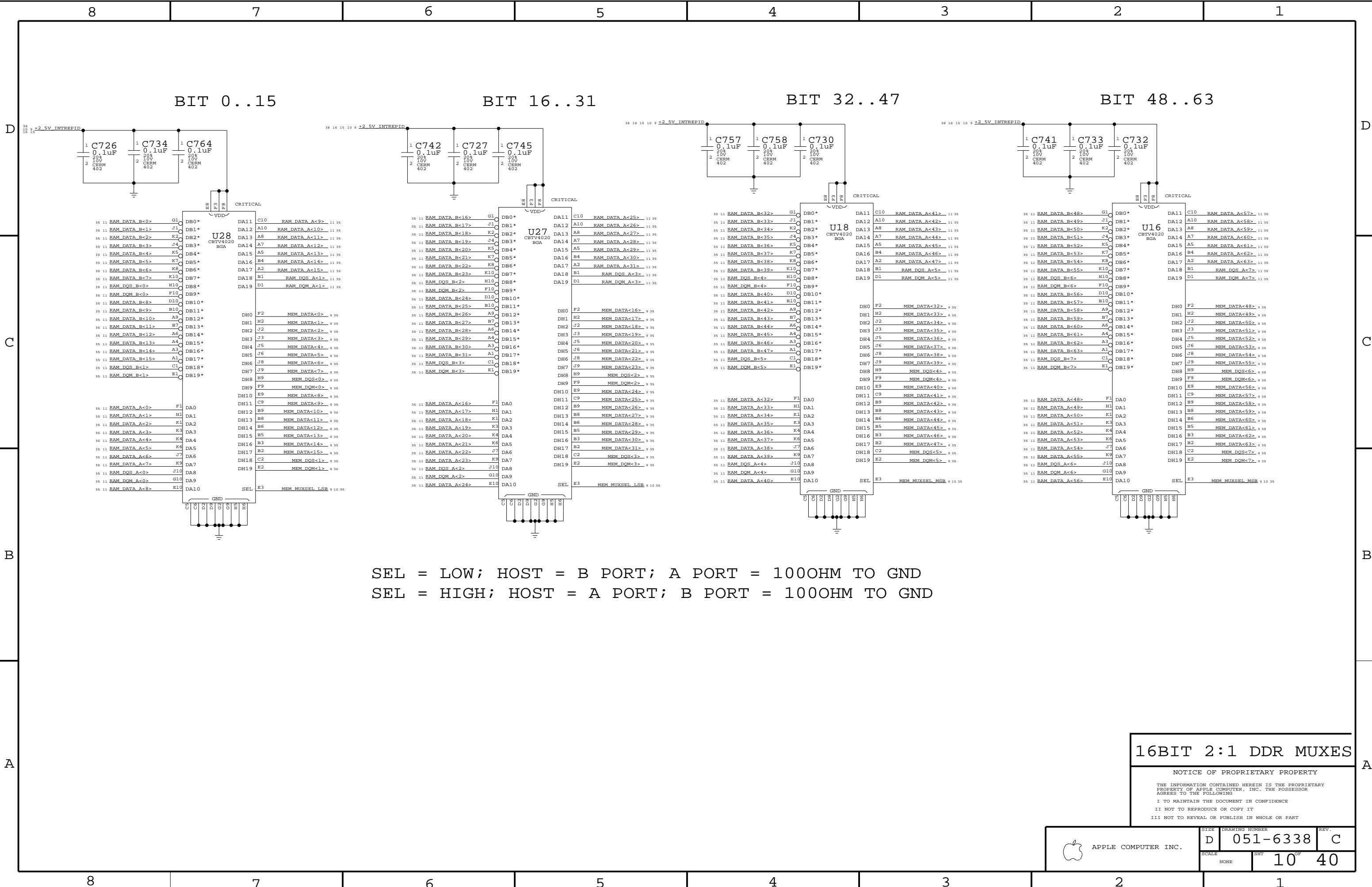
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16BIT 2:1 DDR MUXES

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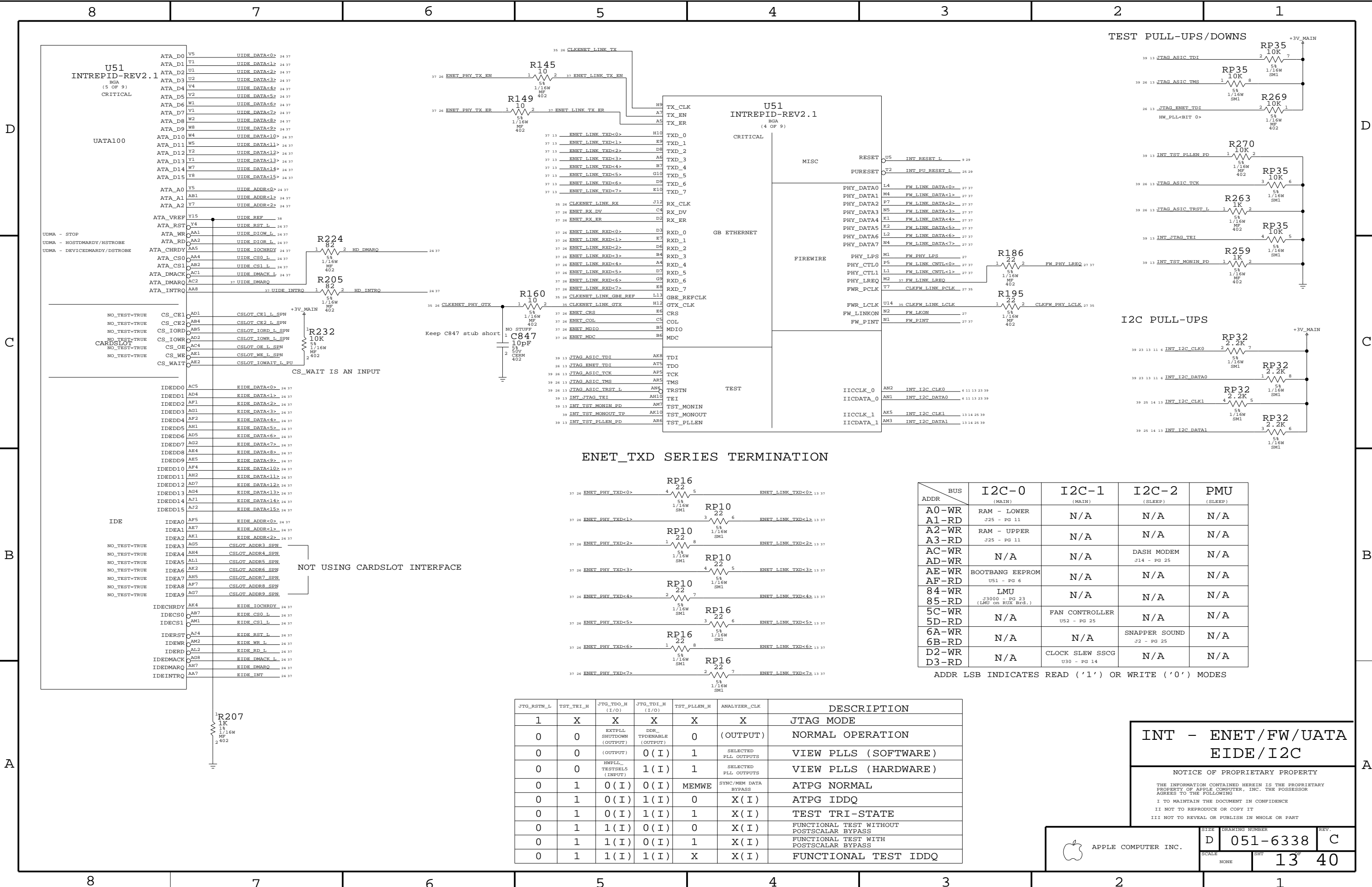
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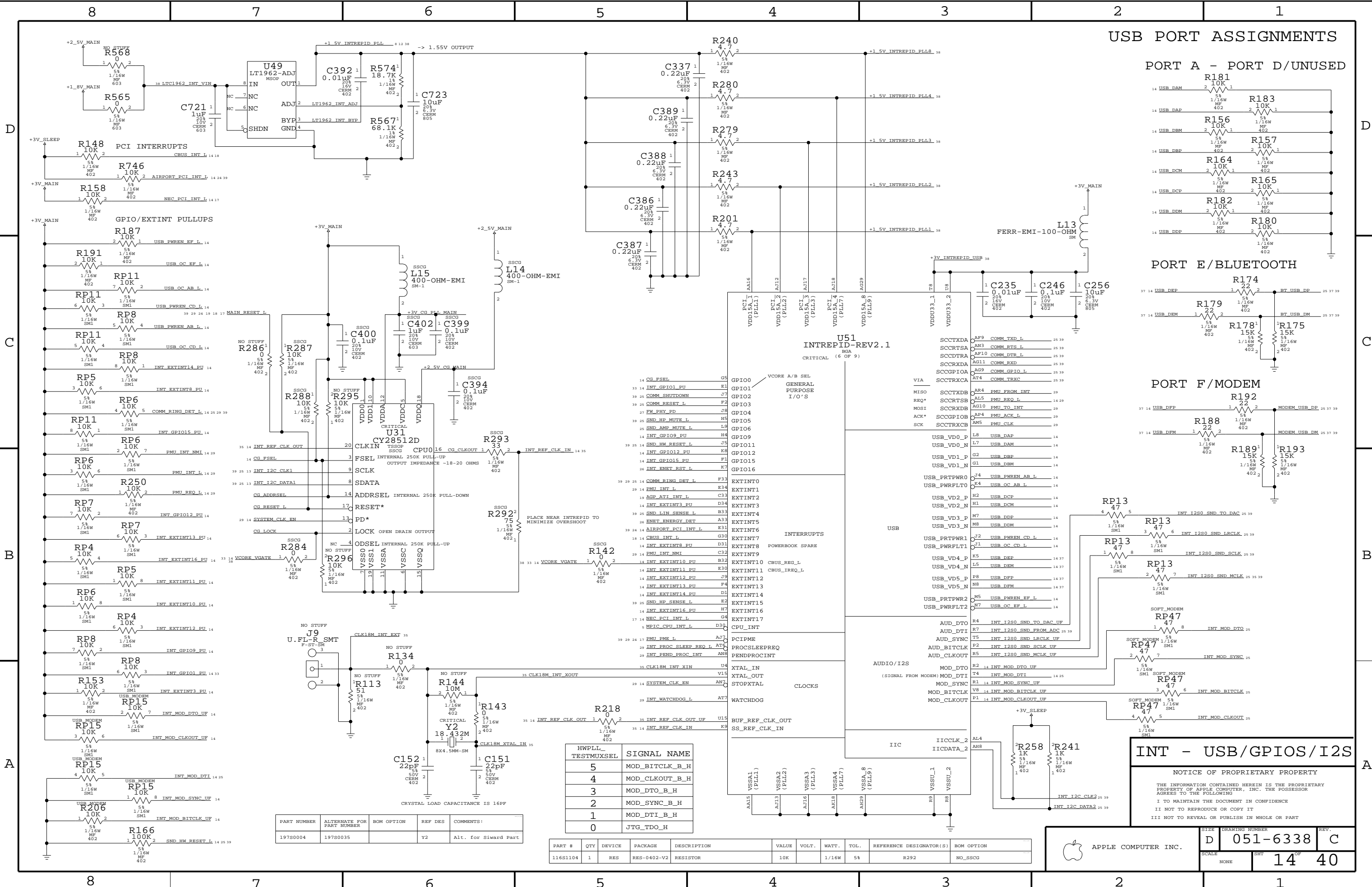
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SHT

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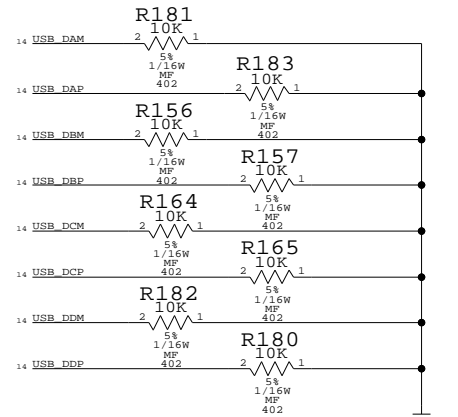
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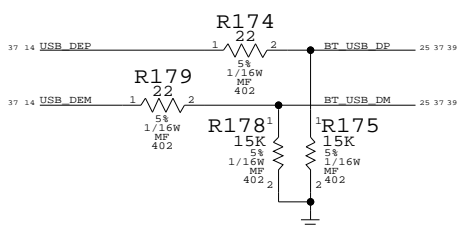


USB PORT ASSIGNMENTS

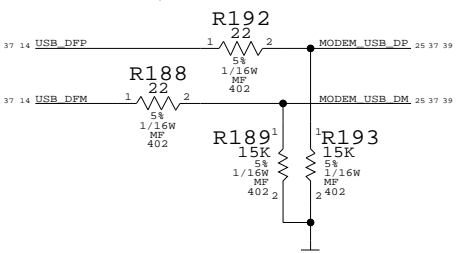
PORT A - PORT D/UNUSED



PORT E/BLUETOOTH



PORT F/MODEM



INT - USB/GPIOS/I2S

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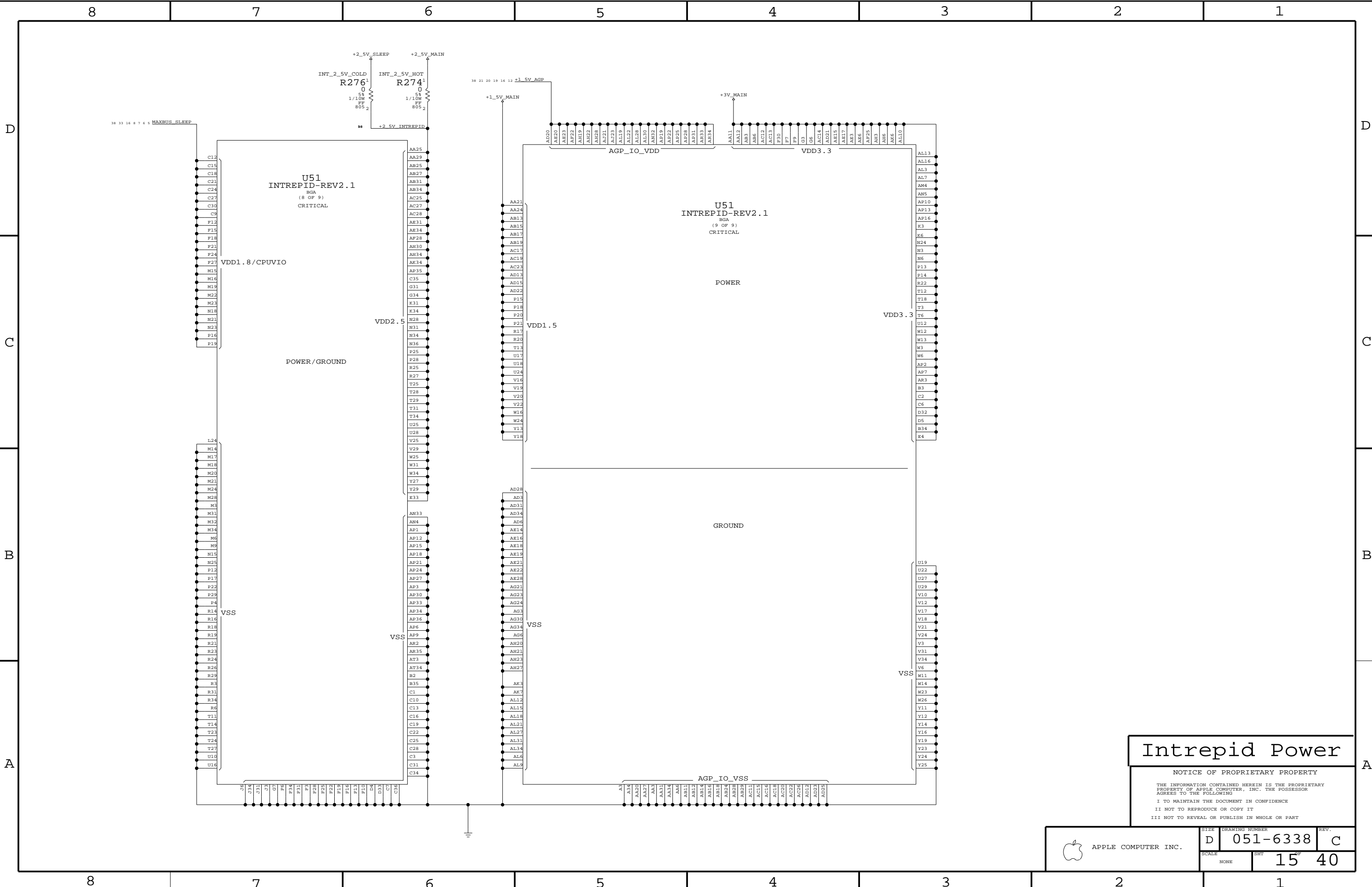
HWPLL TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
19780004	19780035		Y2	Alt. for Siward Part

 APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE	SHT	14 OF 40



Intrepid Power

NOTICE OF PROPRIETARY PROPERTY

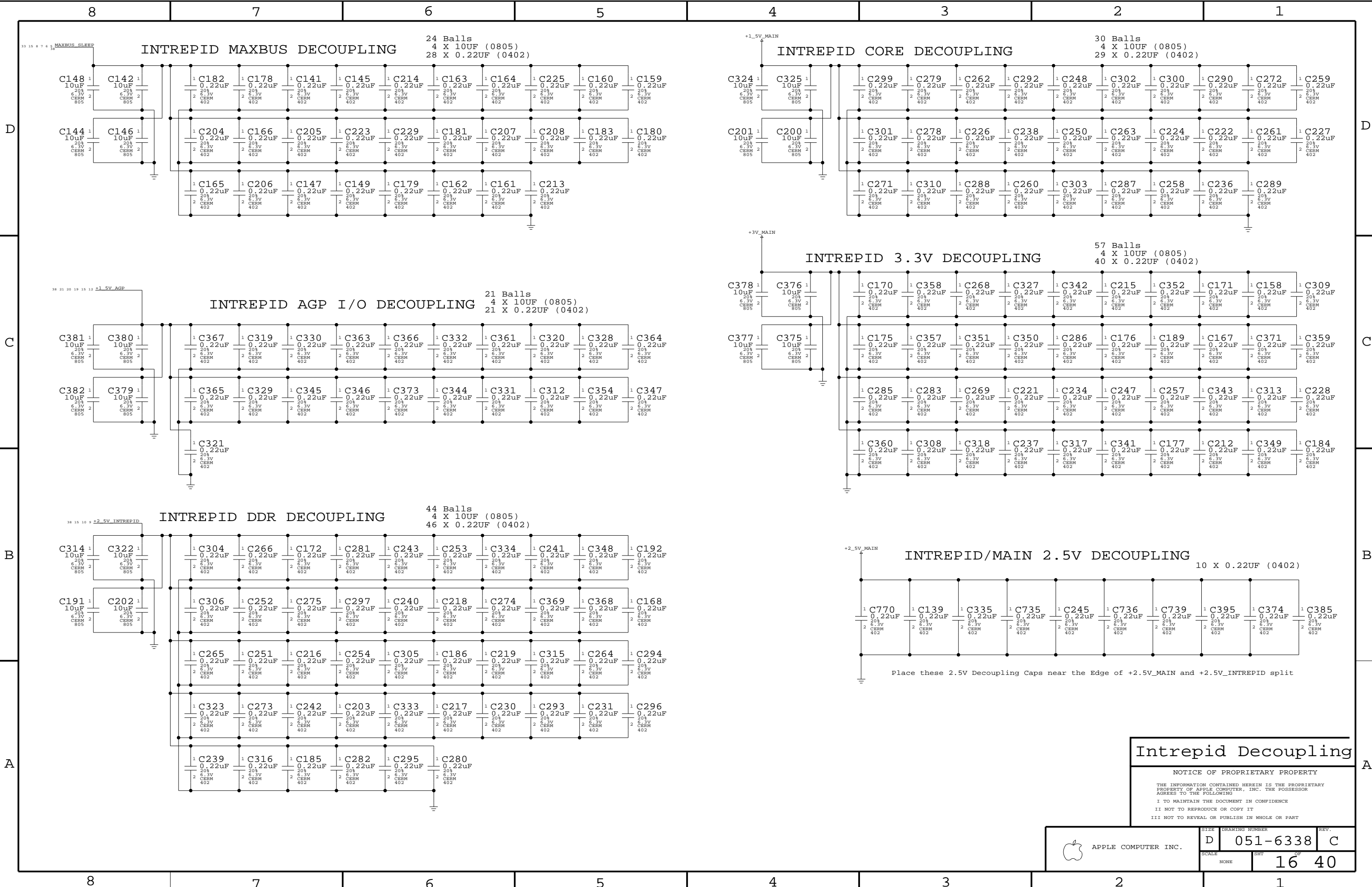
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6338	C
SCALE	SHT		OF
	NONE		15 40



Intrepid Decoupling

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APPLE COMPUTER INC.

SIZE DRAWING NUMBER

D

051-6338

REV.

C

SCALE

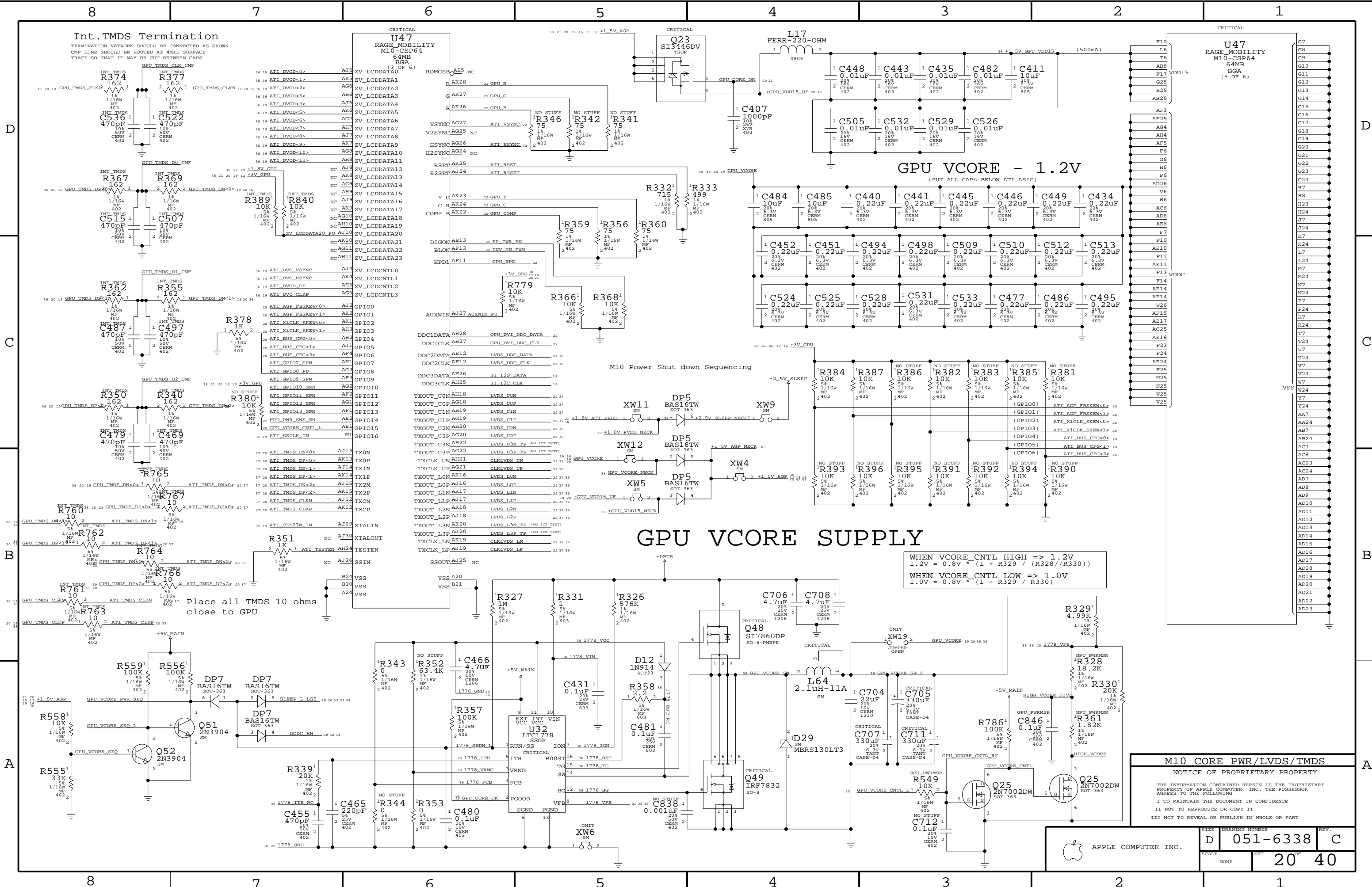
NONE

SHT

OF

16

40



Int.TMDS Termination

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMP LINE SHOULD BE ROUTED AS ANTL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

CRITICAL
U47
RAGE MOBILITY
M10-CSP64
64MB
BGA
(5 OF 6)

CRITICAL
Q23
SI3446DV
T50P

CRITICAL
U47
RAGE MOBILITY
M10-CSP64
64MB
BGA
(5 OF 6)

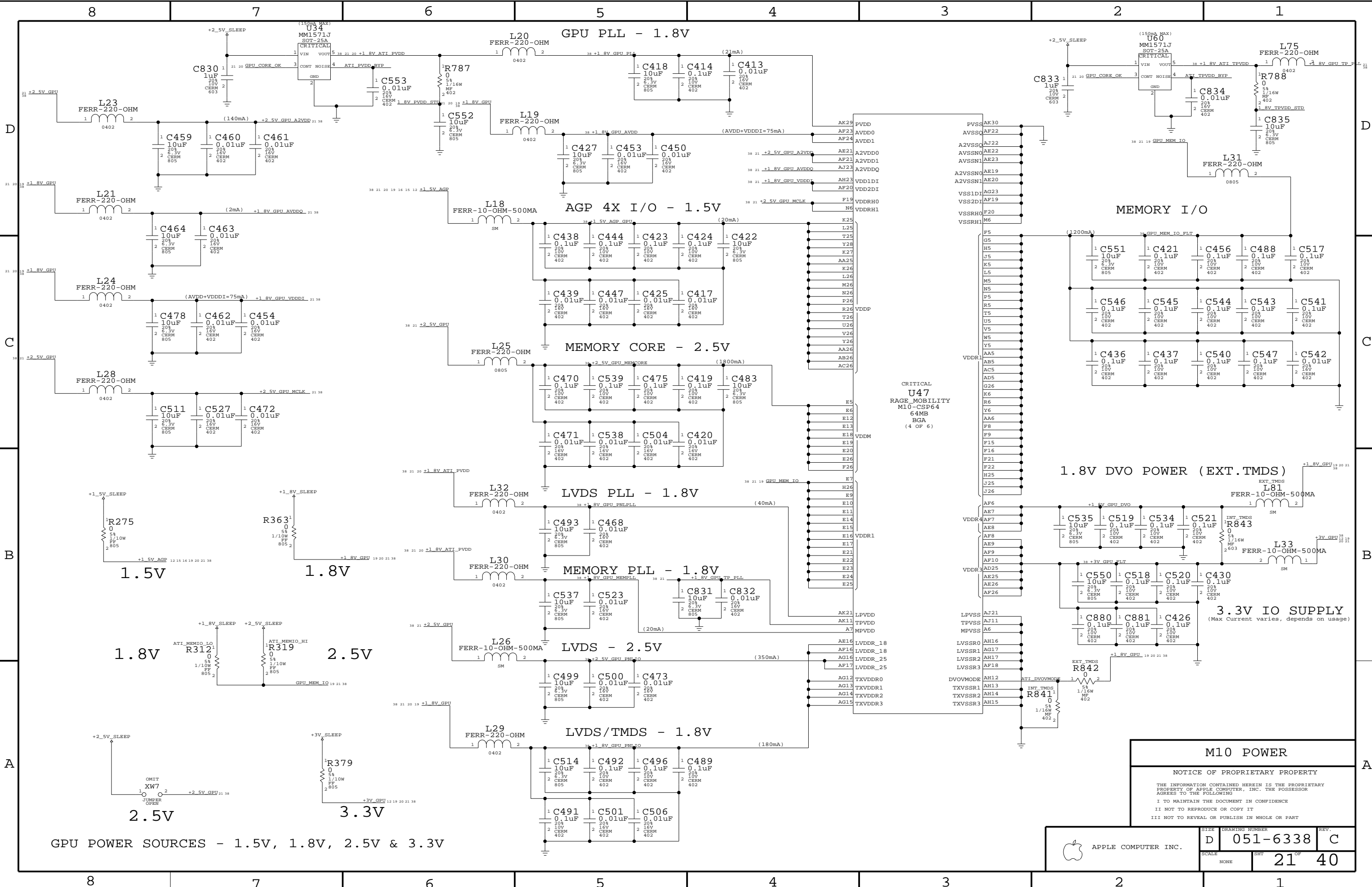
GPU VCORE - 1.2V
(PUT ALL CAPS BELOW ATI ASIC)

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)

M10 CORE PWR/LVDS/TMDS
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M10 POWER

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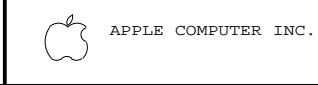
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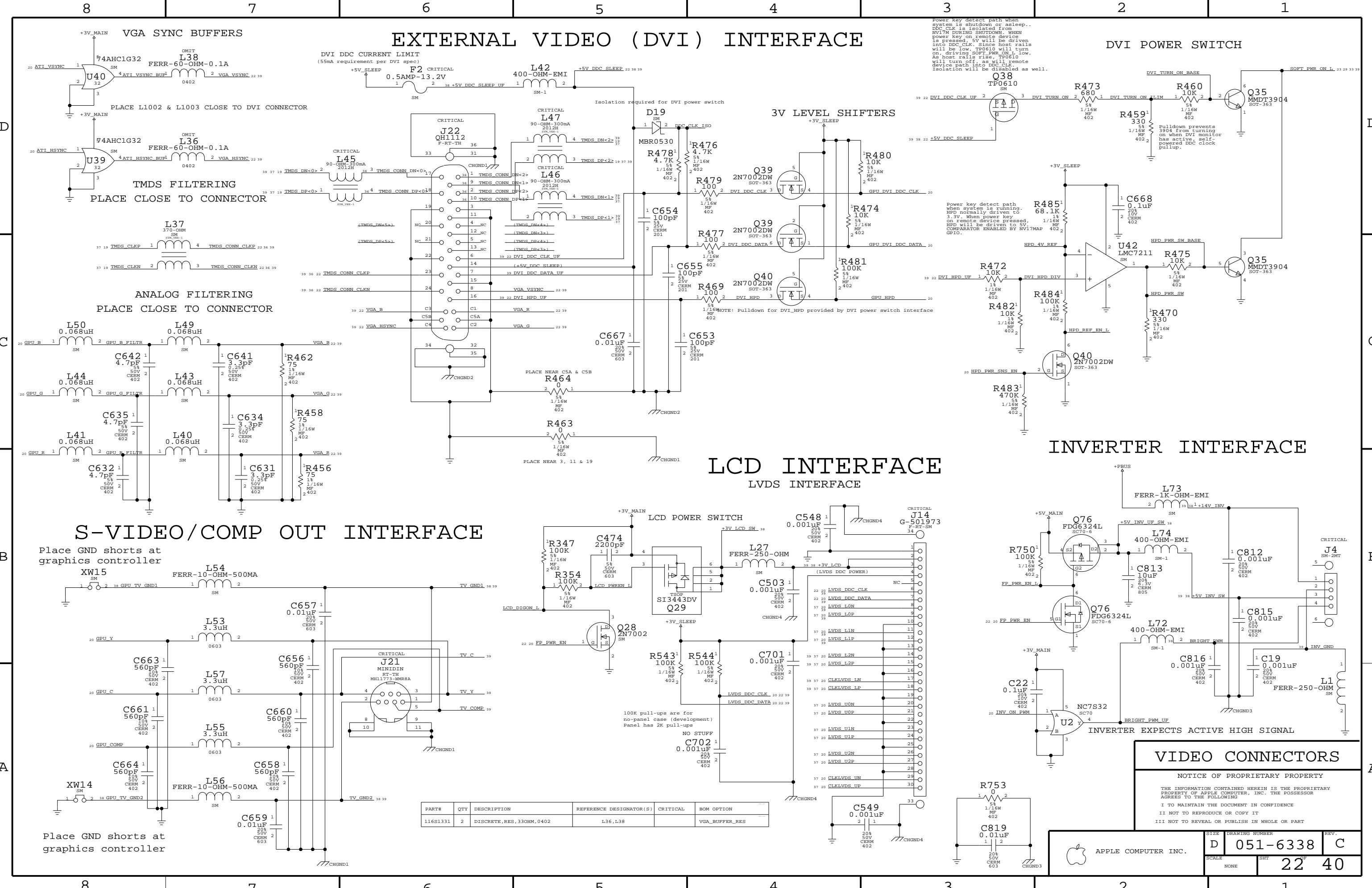
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE	SHT	21 OF 40
NONE		



GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V



VIDEO CONNECTORS

NOTICE OF PROPRIETARY PROPERTY

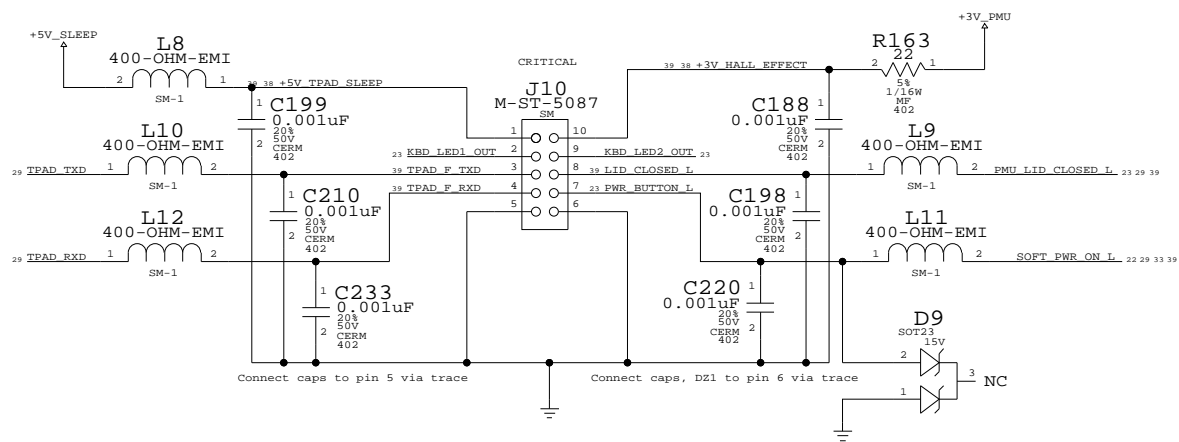
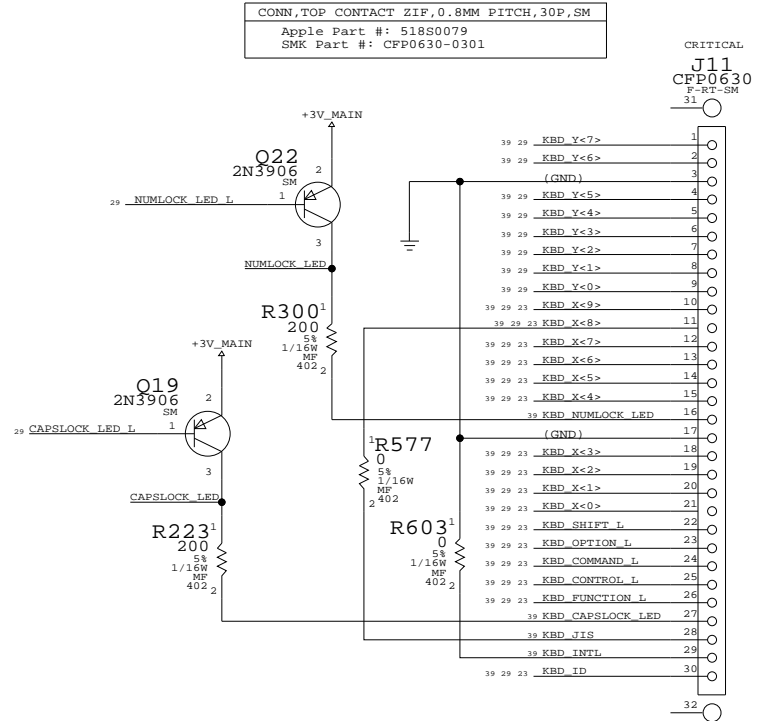
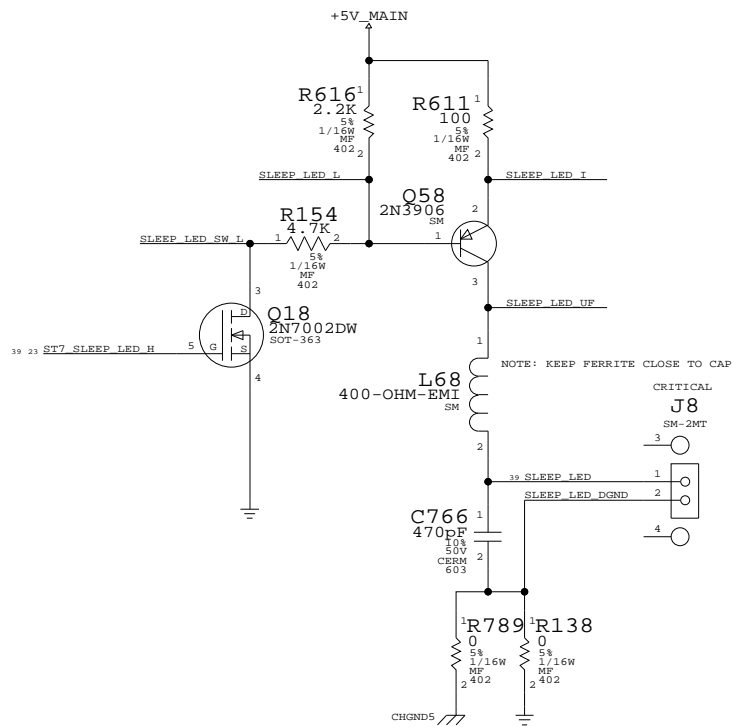
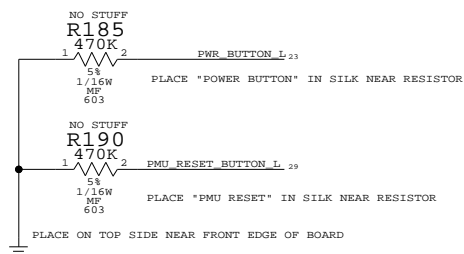
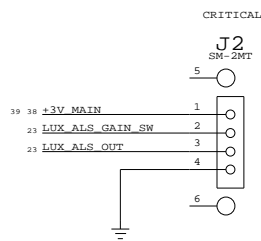
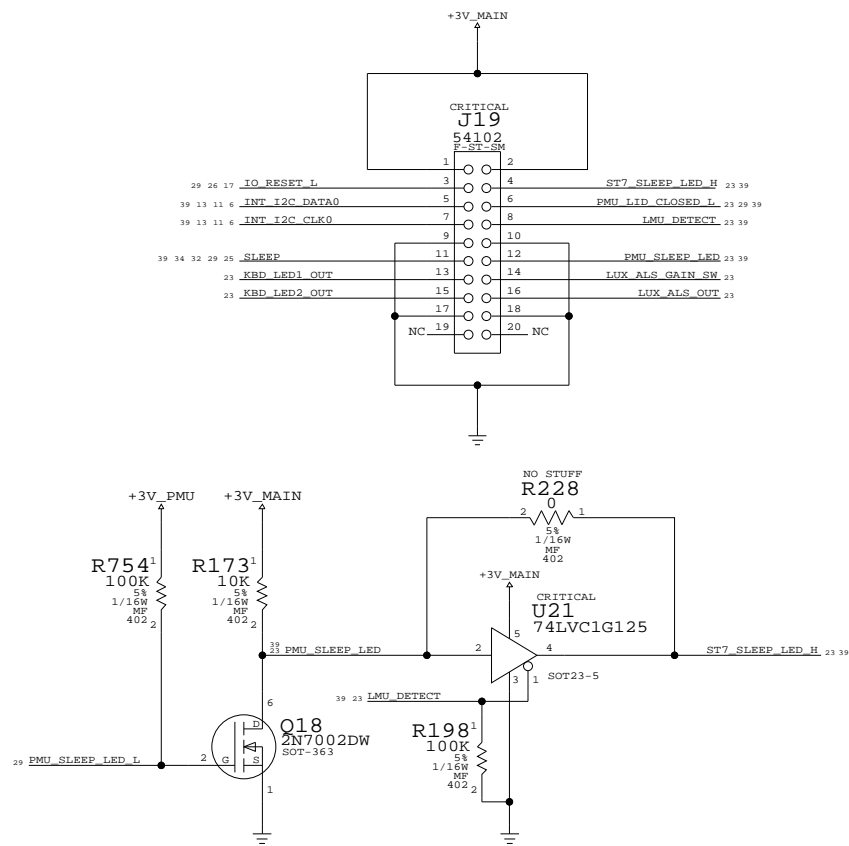
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LEFT I/O & AUDIO BOARD (LIO)

USB MODEM/SOFT MODEM

RIGHT USB BOARD

SERIAL DEBUG INTERFACE

FAN INTERFACE FAN CONTROLLER

FAN/MODEM/SOUND/BACKUP BATT.

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE	SHT	OF
NONE	25	40

D

D

C

C

B

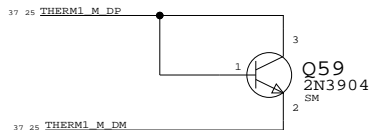
B

A

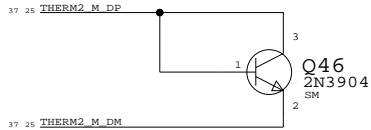
A

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0154	1	CONN,PLUG,0.5MM PITCH,1.5MM STACK,40P,GOLD J3	J3	CRITICAL	?

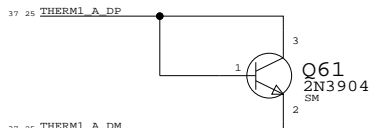
PLACE CLOSE TO CPU
MAIN1



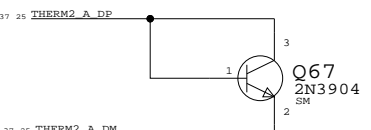
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2



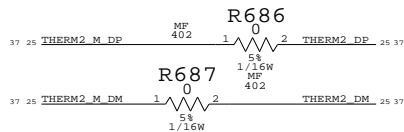
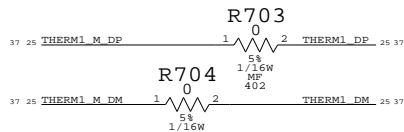
PLACE UNDERNEATH UPPER RAM
ALTERNATE1



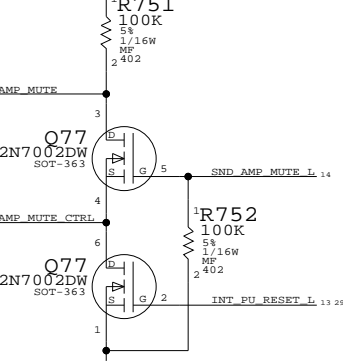
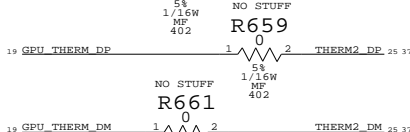
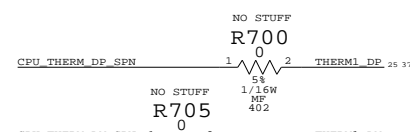
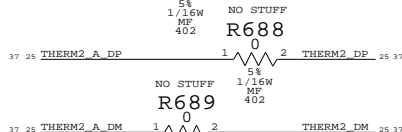
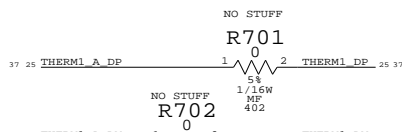
PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



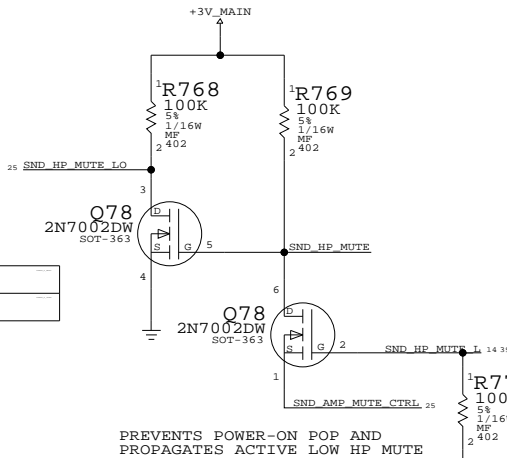
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



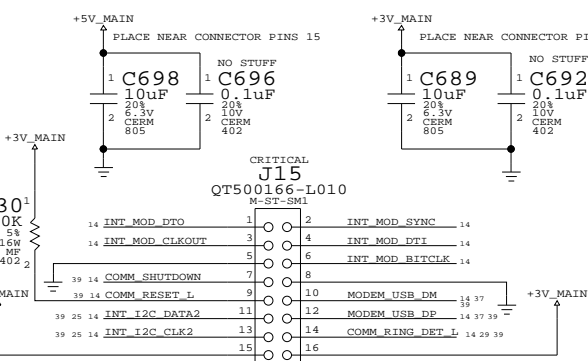
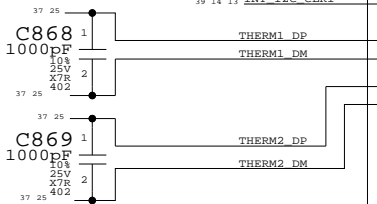
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



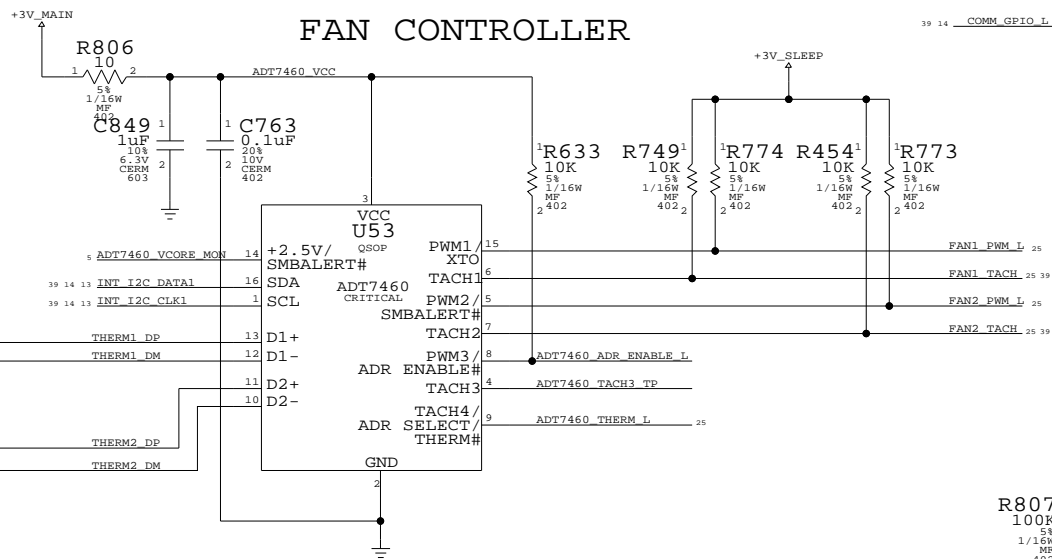
PREVENTS POWER-ON POP AND
GENERATES ACTIVE HIGH SPKR MUTE



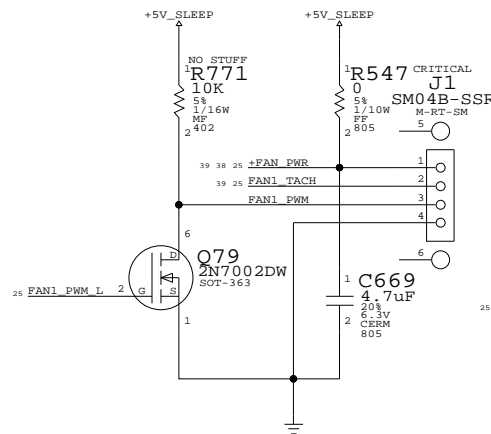
PREVENTS POWER-ON POP AND
PROPAGATES ACTIVE LOW HP MUTE



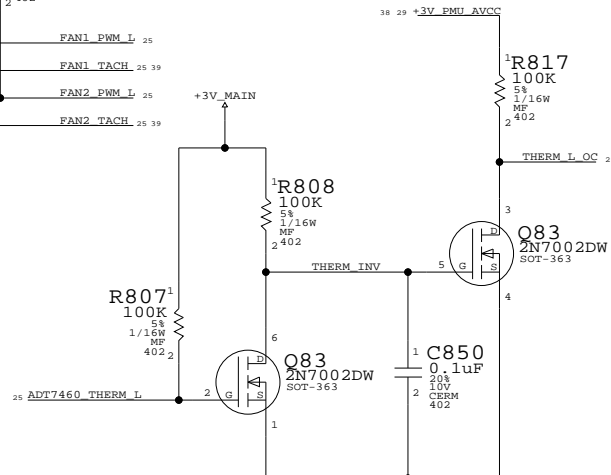
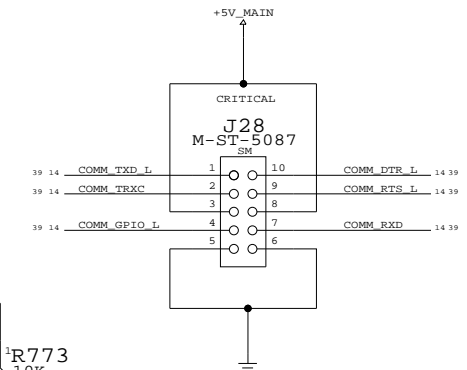
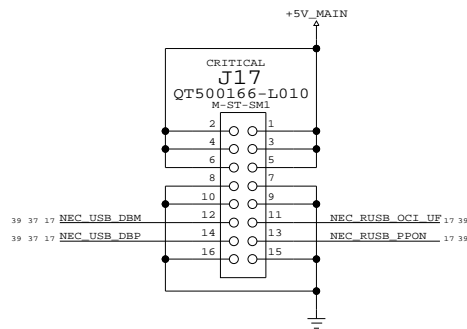
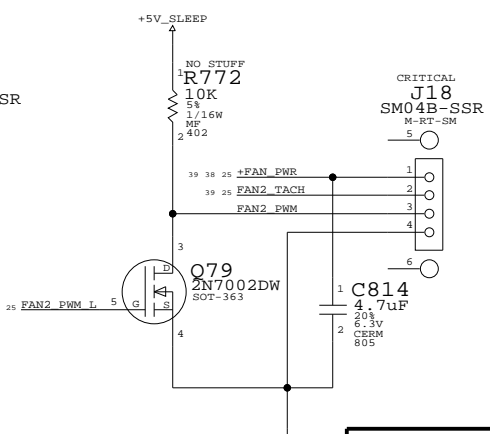
MODEM I2C ADDR ASSIGNED VIA FLEX CABLE

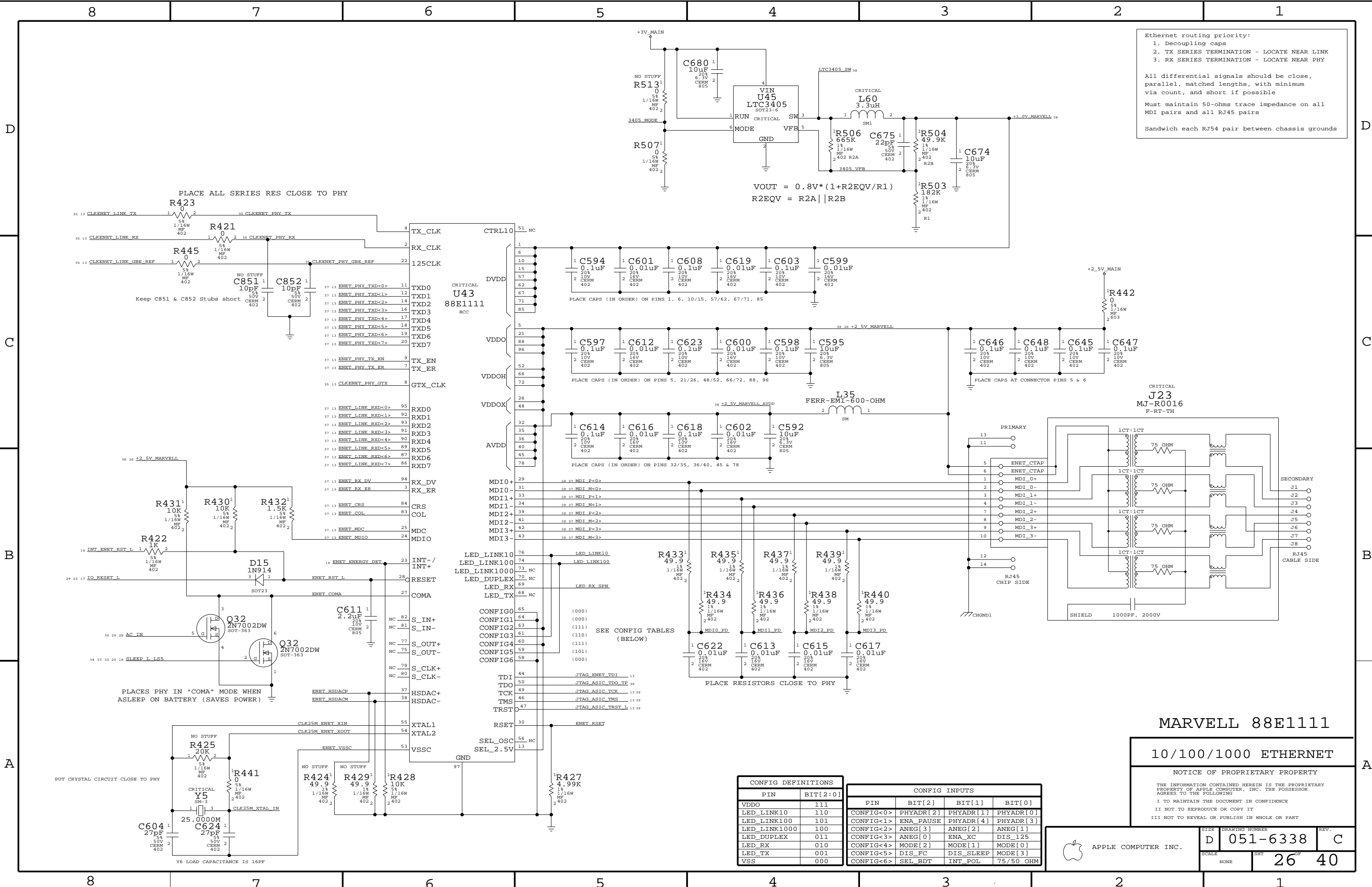


CPU FAN



GPU FAN





Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

MARVELL 88E1111

10/100/1000 ETHERNET

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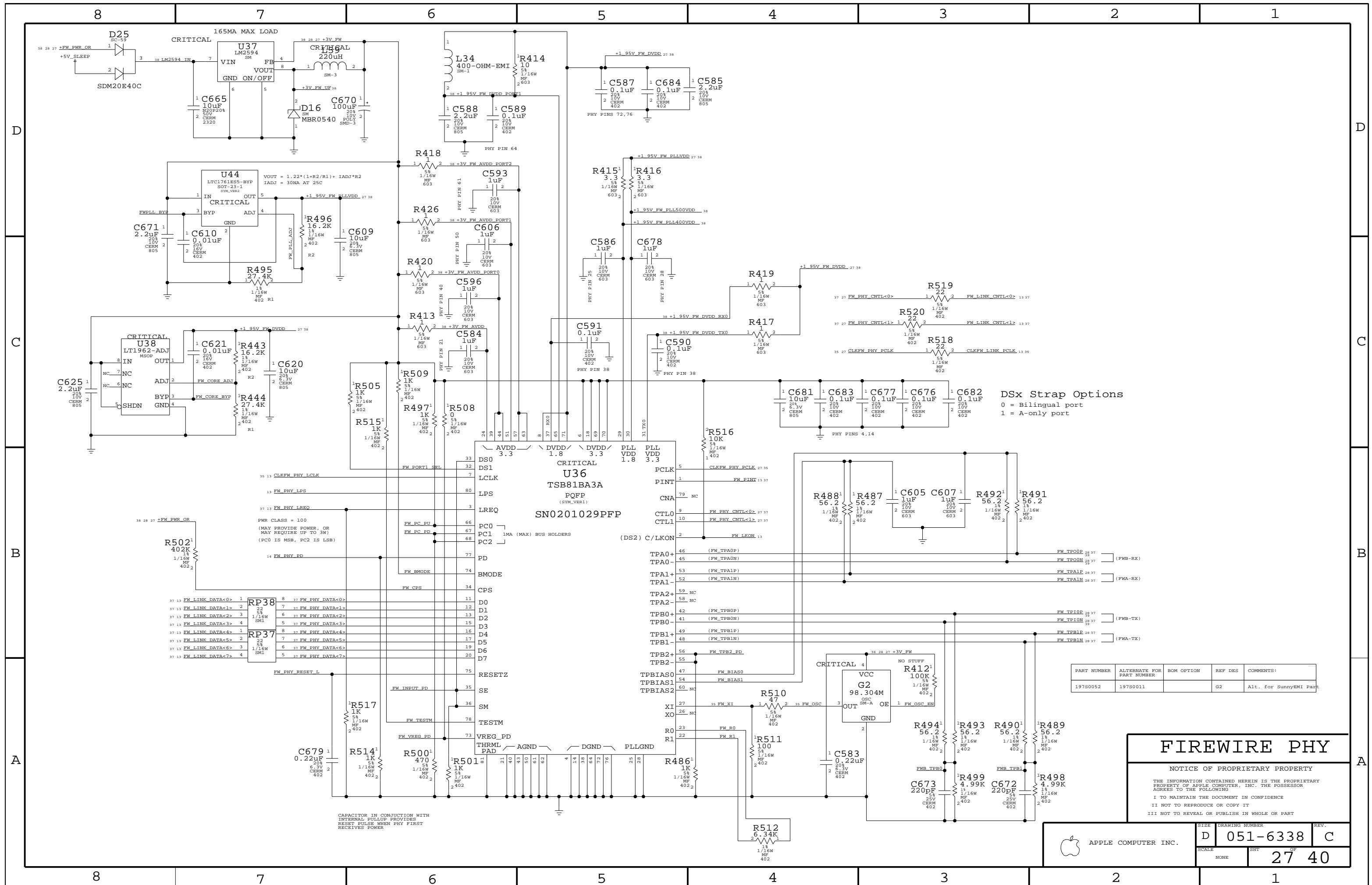
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

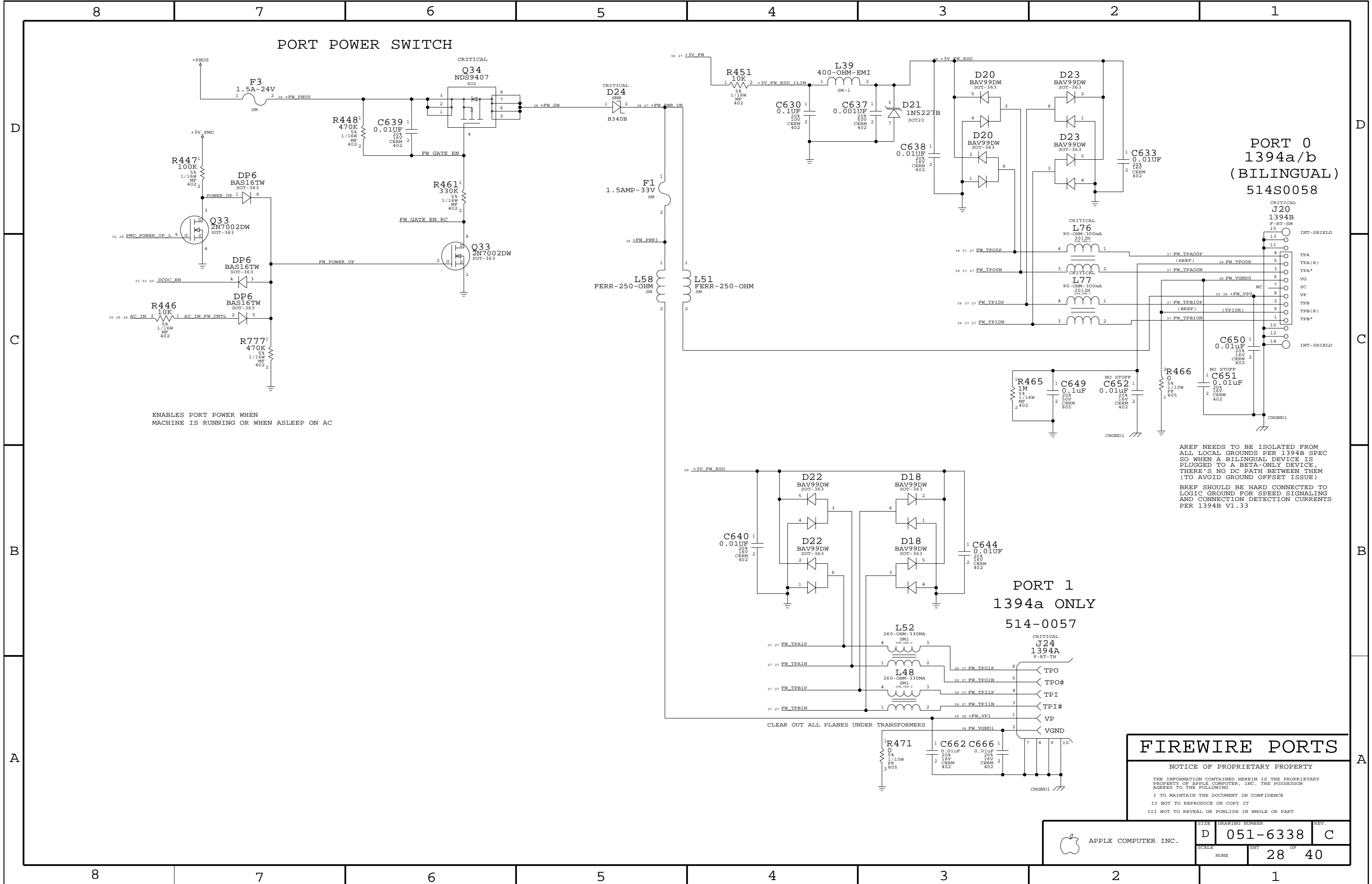


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE	SHT	OF
NONE	26	40

CONFIG DEFINITIONS		CONFIG INPUTS			
PIN	BIT[2:0]	PIN	BIT[2]	BIT[1]	BIT[0]
VDDO	111	CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
LED_LINK10	110	CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
LED_LINK100	101	CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
LED_LINK1000	100	CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
LED_DUPLEX	011	CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
LED_RX	010	CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
LED_TX	001	CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM
VSS	000				





FIREWIRE PORTS

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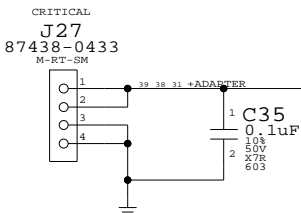
SIZE DRAWING NUMBER REV.

D 051-6338 C

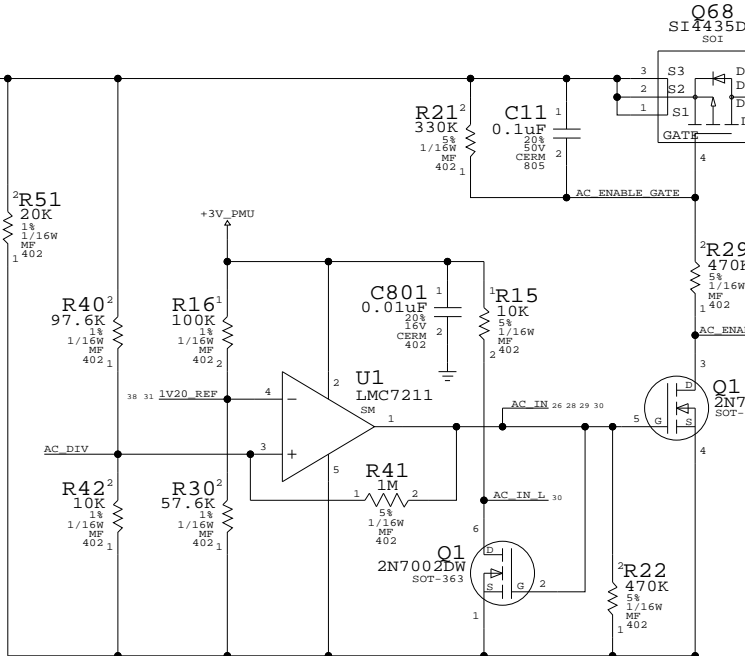
SCALE NONE SHT 28 OF 40

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

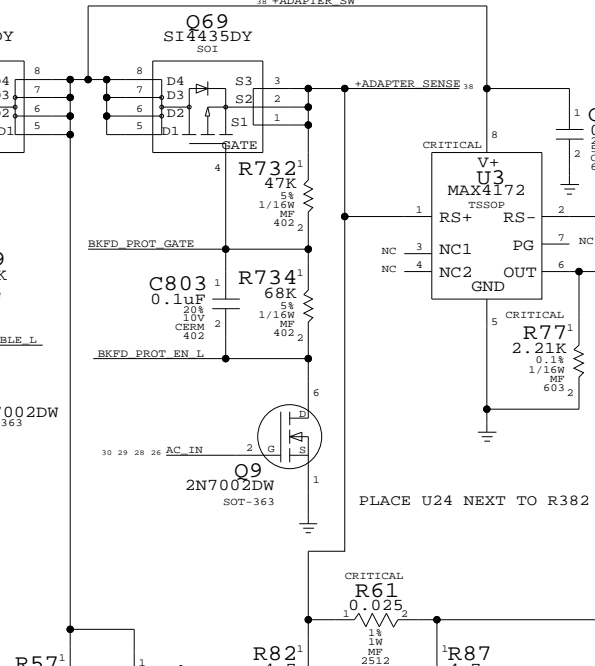


DC INRUSH LIMITER

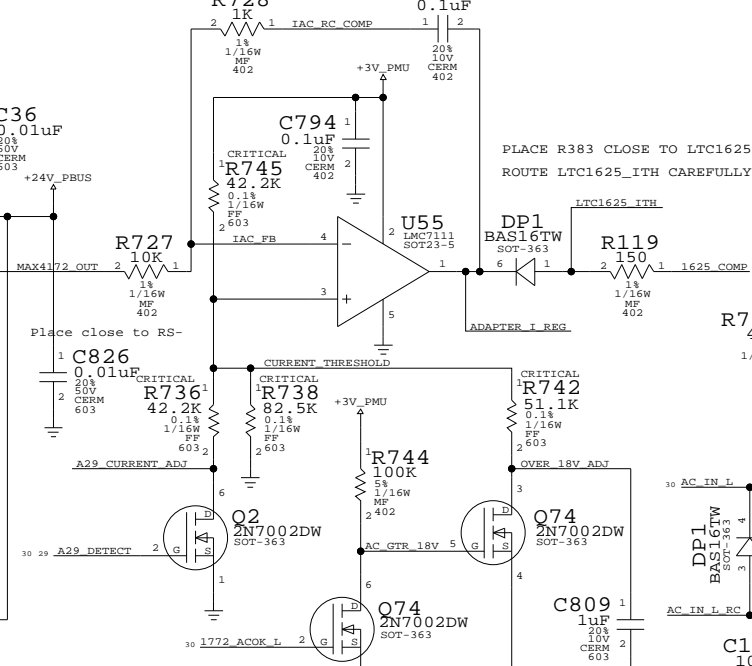


GREATER THAN 13.1V DETECT

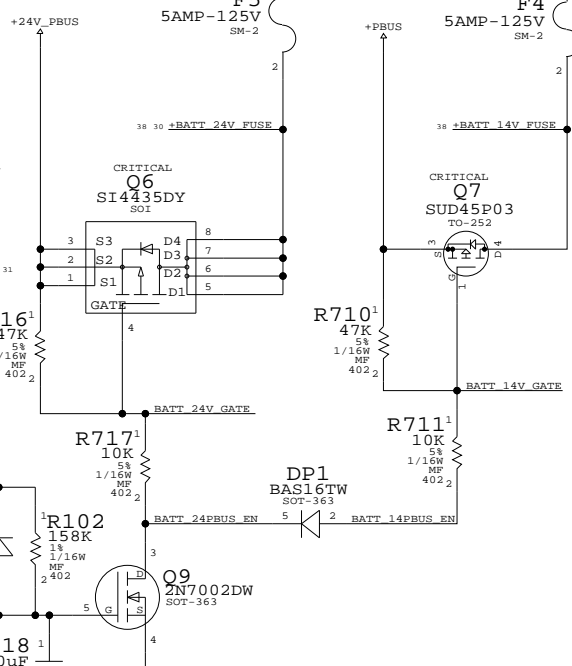
BACKFEED PROTECTION



+PBUS CURRENT LIMIT



BATTERY SWITCH-OVER CIRCUIT

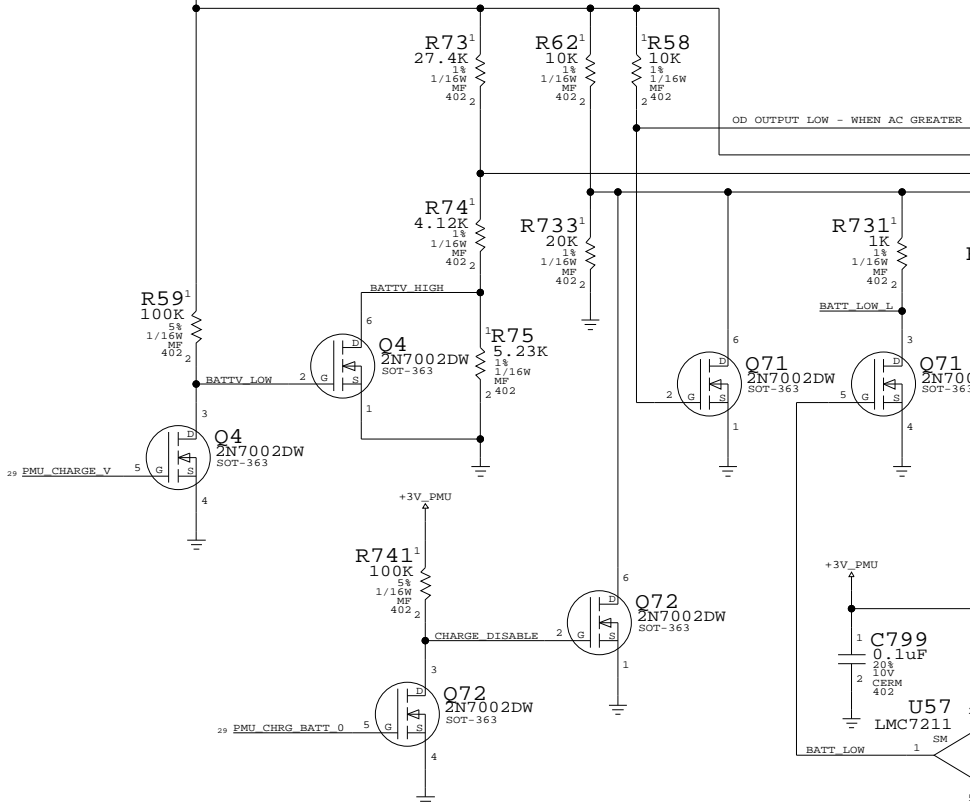


SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE



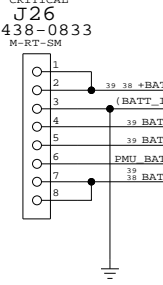
$$V_{BATT} = CELLS \times (4.096 + (0.4096 \times V_{VCTL} / V_{REFIN}))$$

For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN

$$I_{CHG} = (0.2048 / R_{g2}) \times (V_{ICTL} / V_{REFIN})$$

BATTERY CONNECTOR

87438-0833

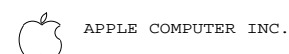


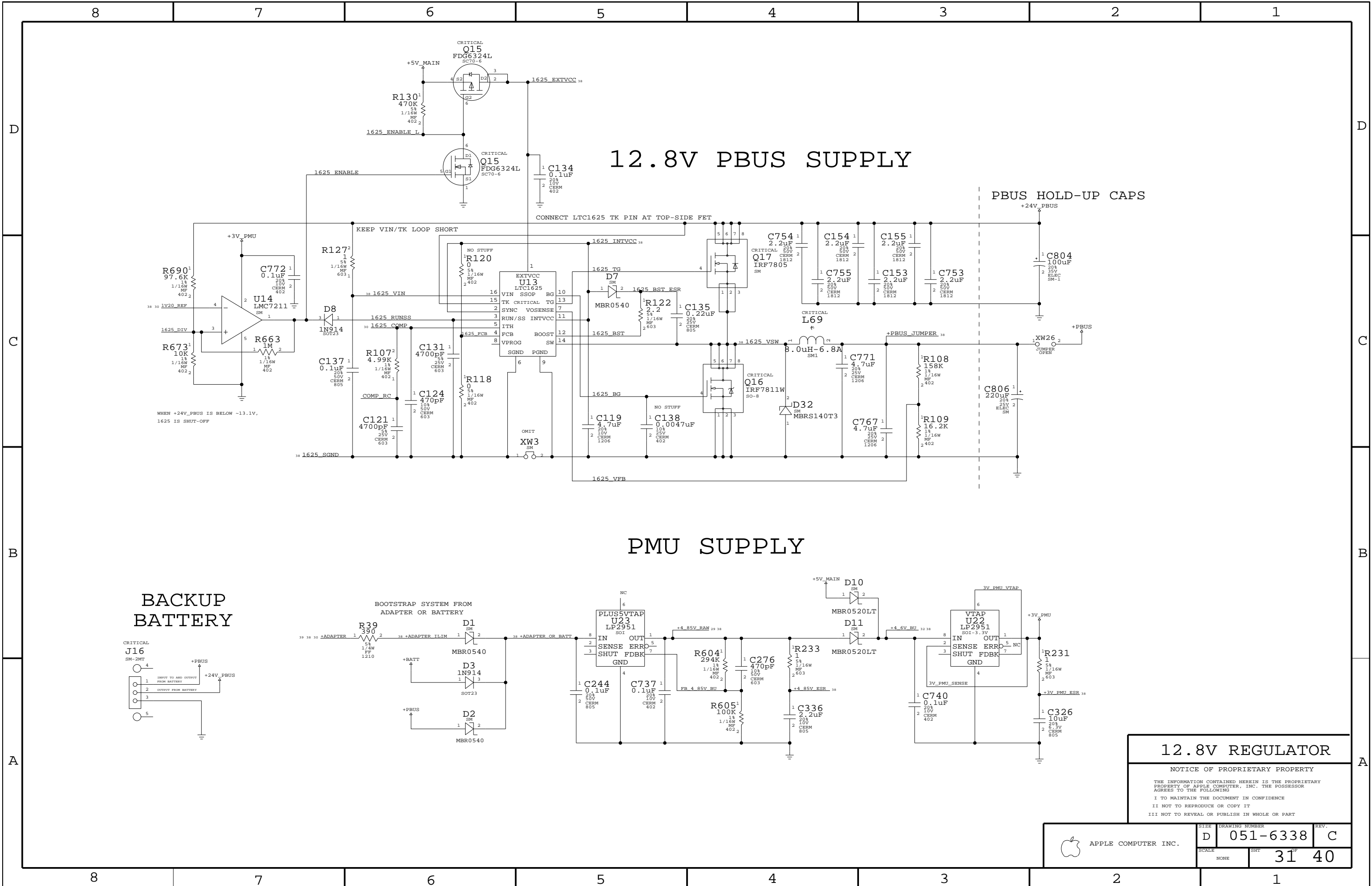
BATTERY CHARGER

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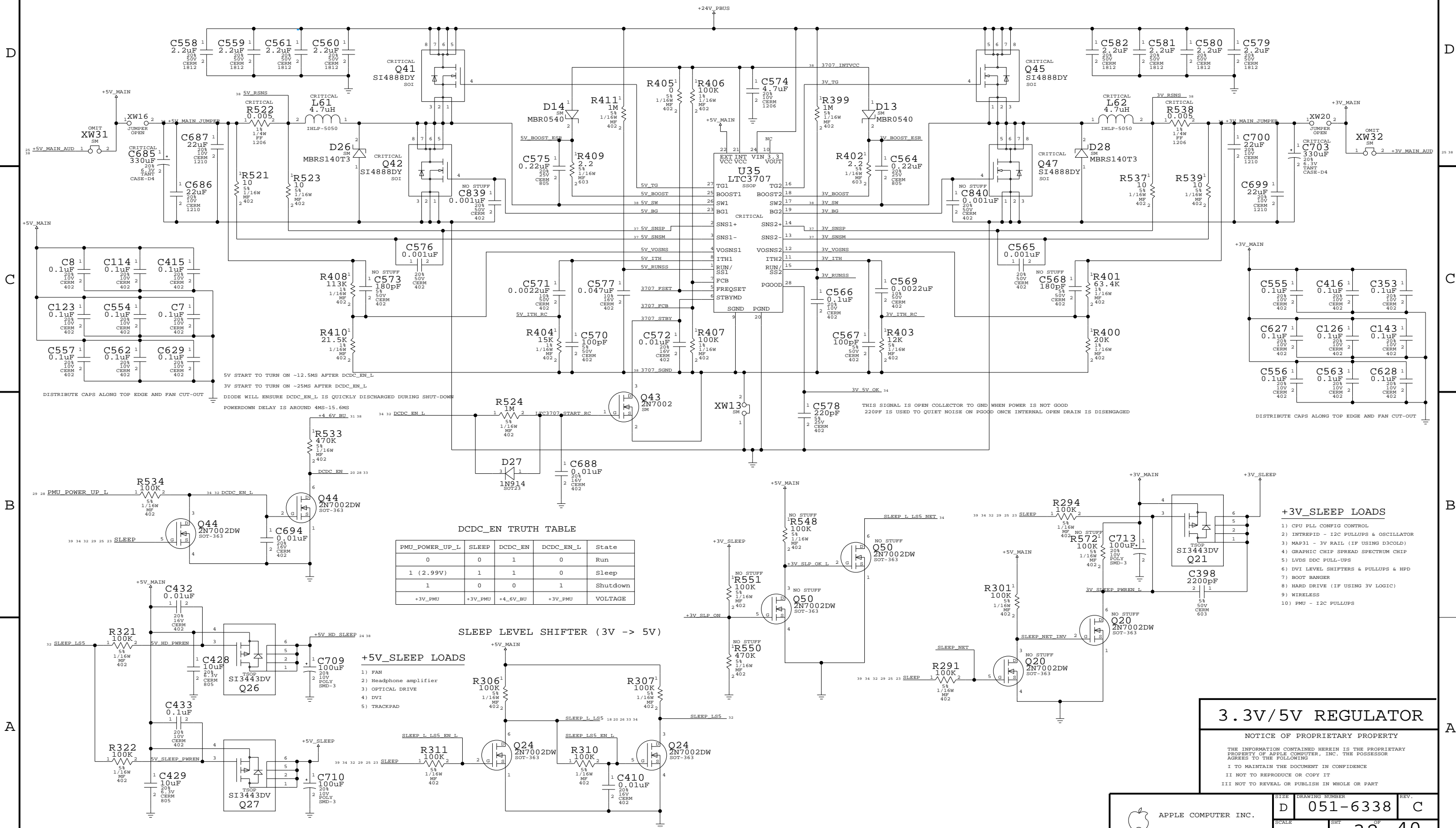
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SCALE	SHT	OF
NONE	30	40





3.3V/5V MAIN SUPPLY



DCDC_EN TRUTH TABLE				
PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4V_BU	+3V_PMU	VOLTAGE

SLEEP LEVEL SHIFTER (3V -> 5V)				
1) FAN	2) Headphone amplifier	3) OPTICAL DRIVE	4) DVI	5) TRACKPAD

3.3V/5V REGULATOR

NOTICE OF PROPRIETARY PROPERTY

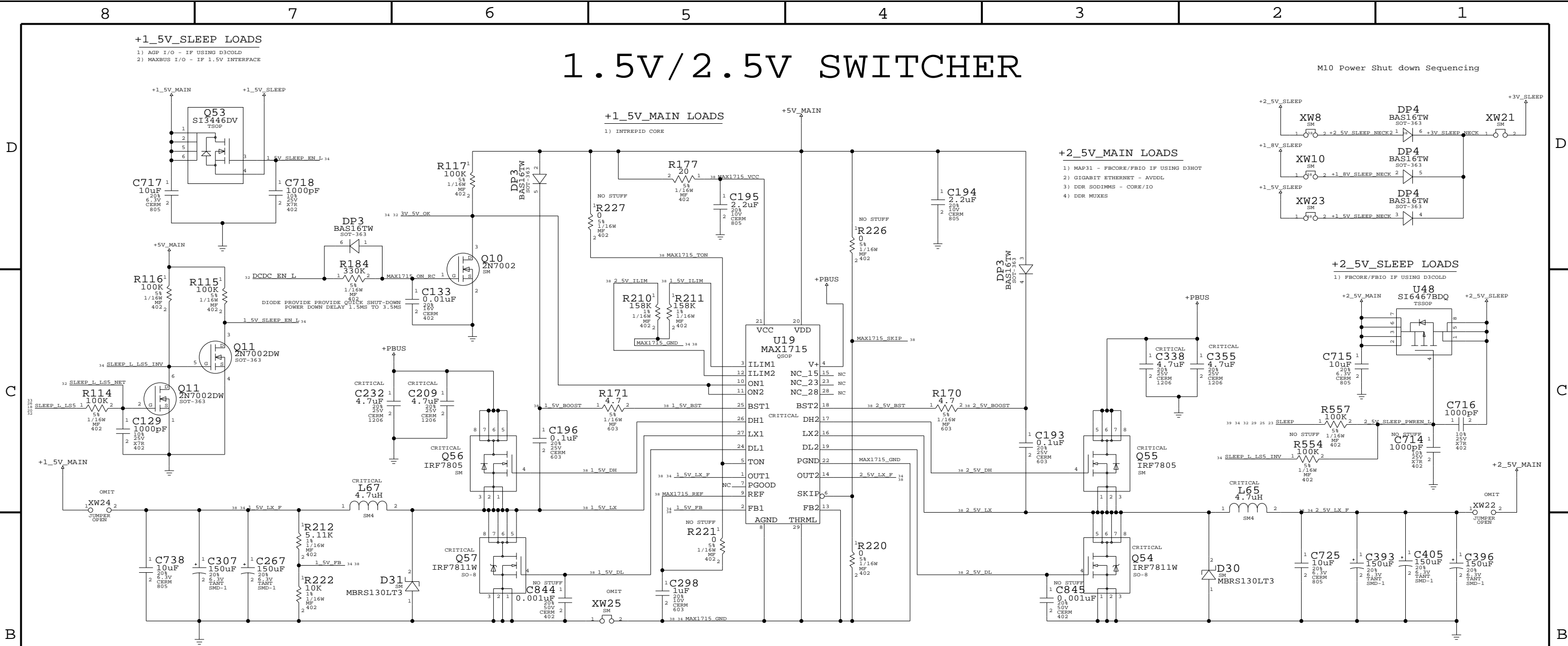
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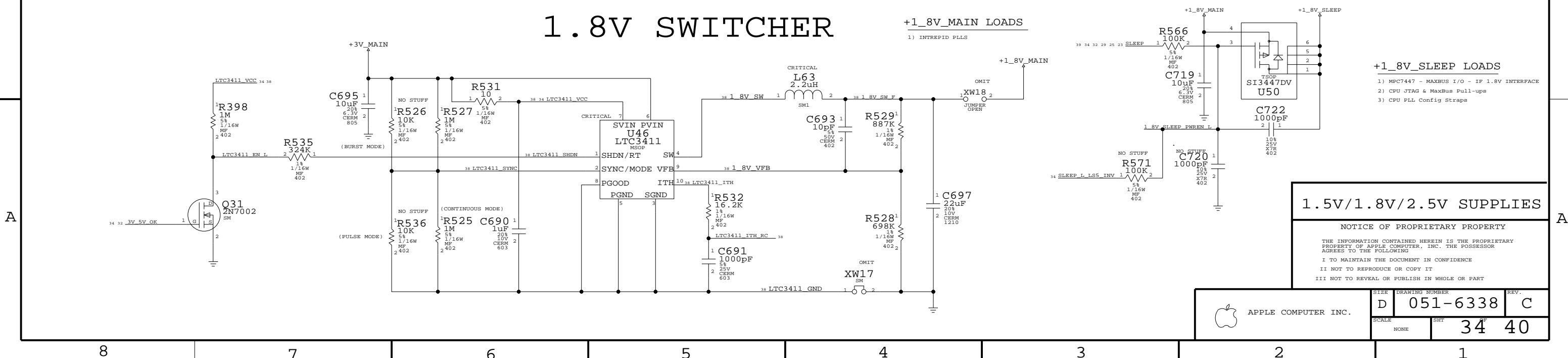
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1.5V/2.5V SWITCHER



1.8V SWITCHER



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APPLE COMPUTER INC.	DRAWING NUMBER		REV.
	D	051-6338	C
SCALE		SHT	40
NONE			

8

7

6

5

4

3

2

1

GROUP

SIG_NAME

PROPAGATION_DELAY

MAX_VIAS

MAX_EXPOSED_LENGTH

STUB_LENGTH

NET_SPACING_TYPE

NO_TEST

PULSE_PARAM

GROUP 0

MEM_DATA<7..0>

1.1S:1602:1700

7

500

(200)

167.0 MHZ

MEM_DATA<0>

1.1S:1602 MTL:1700 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<0>

1.1S:1602 MTL:1700 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<7..0>

1.1S:1903:2000

7

500

(200)

167.0 MHZ

RAM_DATA_A<0>

1.1S:1903 MTL:2000 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<0>

1.1S:1903 MTL:2000 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<7..0>

1.1S:2000:2100

7

500

(200)

167.0 MHZ

RAM_DATA_B<0>

1.1S:2000 MTL:2100 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<0>

1.1S:2000 MTL:2100 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<15..8>

1.1S:1344:1660

7

500

(200)

167.0 MHZ

MEM_DATA<1>

1.1S:1344 MTL:1660 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<1>

1.1S:1344 MTL:1660 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<15..8>

1.1S:1905:2000

7

500

(200)

167.0 MHZ

RAM_DATA_A<1>

1.1S:1905 MTL:2000 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<1>

1.1S:1905 MTL:2000 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<15..8>

1.1S:2004:2412

7

500

(200)

167.0 MHZ

RAM_DATA_B<1>

1.1S:2004 MTL:2412 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<1>

1.1S:2004 MTL:2412 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<23..16>

1.1S:1435:1500

7

500

(200)

167.0 MHZ

MEM_DATA<2>

1.1S:1435 MTL:1500 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<2>

1.1S:1435 MTL:1500 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<23..16>

1.1S:1707:1800

7

500

(200)

167.0 MHZ

RAM_DATA_A<2>

1.1S:1707 MTL:1800 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<2>

1.1S:1707 MTL:1800 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<23..16>

1.1S:1900:2000

7

500

(200)

167.0 MHZ

RAM_DATA_B<2>

1.1S:1900 MTL:2000 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<2>

1.1S:1900 MTL:2000 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<31..24>

1.1S:1233:1485

7

500

(200)

167.0 MHZ

MEM_DATA<3>

1.1S:1233 MTL:1485 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<3>

1.1S:1233 MTL:1485 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<31..24>

1.1S:1700:2165

7

500

(200)

167.0 MHZ

RAM_DATA_A<3>

1.1S:1700 MTL:2165 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<3>

1.1S:1700 MTL:2165 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<25..24>

1.1S:1907:2356

7

500

(200)

167.0 MHZ

RAM_DATA_B<26>

1.1S:1907 MTL:2356 MTL

7

500

(200)

167.0 MHZ

RAM_DATA_B<26>

1.1S:1907 MTL:2356 MTL

7

500

(200)

167.0 MHZ

RAM_DATA_B<31..27>

1.1S:1907:2356

7

500

(200)

167.0 MHZ

RAM_DATA_B<3>

1.1S:1907 MTL:2356 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<3>

1.1S:1907 MTL:2356 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<39..32>

1.1S:1915:2000

7

500

(200)

167.0 MHZ

MEM_DATA<4>

1.1S:1915 MTL:2000 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<4>

1.1S:1915 MTL:2000 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<39..32>

1.1S:1205:1387

7

500

(200)

167.0 MHZ

RAM_DATA_A<4>

1.1S:1205 MTL:1387 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<4>

1.1S:1205 MTL:1387 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<39..32>

1.1S:1404:1686

7

500

(200)

167.0 MHZ

RAM_DATA_B<4>

1.1S:1404 MTL:1686 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<4>

1.1S:1404 MTL:1686 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<47..40>

1.1S:1719:1893

7

500

(200)

167.0 MHZ

MEM_DATA<5>

1.1S:1719 MTL:1893 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<5>

1.1S:1719 MTL:1893 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<47..40>

1.1S:1607:1898

7

500

(200)

167.0 MHZ

RAM_DATA_A<5>

1.1S:1607 MTL:1898 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<5>

1.1S:1607 MTL:1898 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<47..40>

1.1S:1716:2102

7

500

(200)

167.0 MHZ

RAM_DATA_B<6>

1.1S:1716 MTL:2102 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<6>

1.1S:1716 MTL:2102 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<55..48>

1.1S:2101:2170

7

500

(200)

167.0 MHZ

MEM_DATA<6>

1.1S:2101 MTL:2170 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<6>

1.1S:2101 MTL:2170 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<55..48>

1.1S:1204:1357

7

500

(200)

167.0 MHZ

RAM_DATA_A<6>

1.1S:1204 MTL:1357 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<6>

1.1S:1204 MTL:1357 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<55..48>

1.1S:1400:1546

7

500

(200)

167.0 MHZ

RAM_DATA_B<6>

1.1S:1400 MTL:1546 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_B<6>

1.1S:1400 MTL:1546 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<63..56>

1.1S:1611:1696

7

500

(200)

167.0 MHZ

MEM_DATA<7>

1.1S:1611 MTL:1696 MTL

7

500.0000

(200)

167.0 MHZ

MEM_DATA<7>

1.1S:1611 MTL:1696 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<63..56>

1.1S:1809:1887

7

500

(200)

167.0 MHZ

RAM_DATA_A<7>

1.1S:1809 MTL:1887 MTL

7

500.0000

(200)

167.0 MHZ

RAM_DATA_A<7>

1.1S:1809 MTL:1887 MTL

7

500.0000

(200)

167.0 MHZ

MEM_ADDR<12..0>

1.1S:1500

4

(200)

83 MHZ

MEM_ADDR<12..0>

1.1S:2000:3000

10

(200)

MEM_ADDR<1..0>

1.1S:1500

4

(200)

MEM_ADDR<1..0>

1.1S:2000:3000

8

(200)

MEM_CS_L<3..0>

1.1S:1500

4

(200)

MEM_CS_L<3..0>

1.1S:2500:3200

7

(200)

MEM_CKE<3..0>

1.1S:1500

4

(200)

MEM_CKE<3..0>

1.1S:2500:3200

7

(200)

MEM_RAS_L

1.1S:1500 MTL

4

(200)

MEM_RAS_L

1.1S:2000 MTL:4100 MTL

7

(200)

MEM_CAS_L

1.1S:1500 MTL

4

(200)

MEM_CAS_L

1.1S:2000 MTL:4100 MTL

7

(200)

MEM_WE_L

1.1S:1500 MTL

4

(200)

MEM_WE_L

1.1S:2000 MTL:3100 MTL

8

(200)

MEM_MUXSEL_MSB

1.1S:1700 MTL:3000 MTL

8

MEM_MUXSEL_LSB

1.1S:1700 MTL:3000 MTL

7

STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2

TOTAL LENGTH CONTROLLED BY SPREADSHEET

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[illegible][illegible]

8	7	6	5	4	3	2	1
POWER NET CONSTRAINTS							
D	MAIN/SLEEP	GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
			+24V FBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
			+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+5V MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+5V SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+3V MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 39
			+3V SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
			+3V PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+2.5V MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
C	ADAPTER		+2.5V SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+1.8V MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
			+1.8V SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+1.5V MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+1.5V SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+1.5V LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+1.5V SLEEP VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 31 39
			+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	38
			+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	38
B	BATTERY CHARGER		+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
			+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
			BATT_NG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
			1772 DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		30
			1772 LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
			+BATT_14V FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
			+BATT_24V FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
			+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
			+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	30
			1772 LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
A	PMU		1772 PLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
			1772 GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		30
			+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
			+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
			+4.85V RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31
			+4.6V BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		31 32
			+4.85V ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31
			+3V PMU ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		31
			+3V PMU AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 29
			+5V HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 32
A	MISC HD		+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
			+5V TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
			+3V HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
			+14V INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
			+5V INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
			+5V INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
			+5V DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
			+5V DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
			+3V LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22 39
			+3V LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
A	VIDEO		GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.
FUNC_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND
LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
SCAN/TEST	JTAG ASIC TMS	TRUE		13 26
	JTAG ASIC TDI	TRUE		13
	JTAG ASIC TDO TP	TRUE		26
	JTAG ASIC TCK	TRUE		13 26
	JTAG ASIC TRST L	TRUE		13 26
	CPU CHKSTP_OUT_L	TRUE		5
	CPU SRESET_L	TRUE		5
	CPU HRESET_L	TRUE		5 6 7
	JTAG CPU TMS	TRUE		5 6
	JTAG CPU TDI	TRUE		5 6
	JTAG CPU TDO TP	TRUE		5
	JTAG CPU TCK	TRUE		5 6
	JTAG CPU TRST L	TRUE		5 6
	INT_JTAG_TDI	TRUE		13
	INT_TST_MONIN_PD	TRUE		13
	INT_TST_MONOUT_TP	TRUE		13
	INT_TST_PLEEN_PD	TRUE		13
	INT_I2C_CLK0	TRUE		6 11 13 23
	INT_I2C_DATA0	TRUE		6 11 13 23
	INT_I2C_CLK1	TRUE		13 14 25
INT I2C	INT_I2C_DATA1	TRUE		13 14 25
PWR/GND	+PBUS	TRUE		38
	+24V_PBUS	TRUE		38
	GPU_VCORE	TRUE		19 20 38
	1778_VFB	TRUE		20 38
	CPU_VCORE_SLEEP	TRUE		5 13 38
	VCORE_FB	TRUE		23 38
	+1_8V_MAIN	TRUE		38
	+2_5V_MAIN	TRUE		38
	+5V_MAIN	TRUE	2	38 39
	+5V_SLEEP	TRUE	2	38 39
CARDBUS	+3V_MAIN	TRUE	4	23 38
				1000
	+3V_PMU	TRUE		38
	CBUS_DET_1_L	TRUE		2000
	CBUS_DET_2_L	TRUE		2000
	TMDS_DM<0...2>	TRUE		1000
	TMDS_DP<0...2>	TRUE		19 22 37
	TMDS_CONN_CLKN	TRUE		1000
	TMDS_CONN_CLKP	TRUE		1000
	VGA_R	TRUE		1000
DVI	VGA_G	TRUE		1000
	VGA_B	TRUE		1000
	VGA_HSYNC	TRUE		1000
	VGA_VSYNC	TRUE		1000
	DVI_DDC_CLK_UP	TRUE		1000
	DVI_DDC_DATA_UP	TRUE		1000
	DVI_HPD_UP	TRUE		1000
	+5V_DDC_SLEEP	TRUE		2000
			2	2000
			6	1000
LVDS	LVDS_L0N	TRUE		1000
	LVDS_L0P	TRUE		1000
	LVDS_L1N	TRUE		1000
	LVDS_L1P	TRUE		1000
	LVDS_L2N	TRUE		1000
	LVDS_L2P	TRUE		1000
	CLKLVDS_LN	TRUE		1000
	CLKLVDS_LP	TRUE		1000
	LVDS_DDC_CLK	TRUE		1000
	LVDS_DDC_DATA	TRUE		1000
INVERTER	+3V_LCD	TRUE	2	2000
	+3V_SLEEP	TRUE	2	2000
			6	1000
	+14V_INV	TRUE		2000
	+5V_INV_SW	TRUE		2000
	BRIGHT_PWM	TRUE		2000
	INV_GND	TRUE		2000
	TV_C	TRUE		1000
	TV_Y	TRUE		2000
	TV_COMP	TRUE		2000
S-VIDEO	TV_GND1	TRUE		2000
	TV_GND2	TRUE		2000
	INT_I2S0_SND_TO_DAC	TRUE		1000
	INT_I2S0_SND_LRCLK	TRUE		1000
	INT_I2S0_SND_MCLK	TRUE		1000
	INT_I2S0_SND_SCLK	TRUE		1000
	INT_I2S0_SND_FROM_ADC	TRUE		1000
	SND_HP_MUTE_L	TRUE		1000
	SND_AMP_MUTE	TRUE		1000
	SND_HW_RESET_L	TRUE		1000
LIO	SND_HP_SENSE_L	TRUE		1000
	SND_LIN_SENSE_L	TRUE		1000
	INT_I2C_CLK2	TRUE		1000
	INT_I2C_DATA2	TRUE		1000
	ADAPTER_DET	TRUE		1000
	CHARGE_LED_L	TRUE		1000
	NEC_LUSB_OCI_UF	TRUE		1000
	NEC_LUSB_PPON	TRUE		1000
	+5V_MAIN	TRUE	2	2000
	+5V_SLEEP	TRUE	2	2000
	+3V_SLEEP	TRUE		2000

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
USB	NEC_USB_DAM	TRUE		17 25 37
	NEC_USB_DAP	TRUE		17 25 37
	NEC_USB_DBM	TRUE		17 25 37
	NEC_USB_DBP	TRUE		17 25 37
	BT_USB_DM	TRUE		14 25 37
	BT_USB_DP	TRUE		14 25 37
	MODEM_USB_DM	TRUE		14 25 37
	MODEM_USB_DP	TRUE		14 25 37
	NEC_RUSB_PPON	TRUE		17 25
	NEC_RUSB_OCI_UF	TRUE		17 25
	PCI_AD<0...31>	TRUE	1000	9 12 17 18 24 37
	PCI_FRAME_L	TRUE	1000	12 17 18 24 37
	PCI_TRDY_L	TRUE	1000	12 17 18 24 37
	PCI_IRDY_L	TRUE	1000	12 17 18 24 37
	PCI_DEVSEL_L	TRUE	1000	12 17 18 24 37
	PCI_STOP_L	TRUE	1000	12 17 18 24 37
	PCI_PAR	TRUE	1000	12 17 18 24 37
	AIRPORT_FCI_REQ_L	TRUE	1000	12 24
	AIRPORT_FCI_GNT_L	TRUE	1000	12 24
	AIRPORT_FCI_INT_L	TRUE	1000	14 24
RT. USB WIRELESS	MAIN_RESET_L	TRUE	1000	14 17 18 19 24 29
	CLK33M_AIRPORT	TRUE	1000	12 24 35
	PMU_PME_L	TRUE	1000	14 17 24 29
	ROM_ONBOARD_CS_L	TRUE	1000	9 24
	ROM_OE_L	TRUE	1000	9 12 24
	ROM_CS_L	TRUE	1000	9 12 24
	ROM_RW_L	TRUE	1000	9 12 24
	RF_DISABLE_L	TRUE	1000	24
	AIRPORT_CLKRUN_L	TRUE	1000	24
	+3V_AIRPORT	TRUE	2000	38
		TRUE	6	1000
OPTICAL	EIDE_OPTICAL_DATA<0...15>	TRUE		2000
	EIDE_OPTICAL_DMA_RQ	TRUE		2000
	EIDE_OPTICAL_READ_L	TRUE		2000
	EIDE_OPTICAL_DMAACK_L	TRUE		2000
	EIDE_OPTICAL_ADDR<0...2>	TRUE		2000
	EIDE_OPTICAL_CS0_L	TRUE		2000
	EIDE_OPTICAL_CSI_L	TRUE		2000
	EIDE_OPTICAL_RST_L	TRUE		2000
	EIDE_OPTICAL_WR_L	TRUE		2000
	EIDE_OPTICAL_IOCHRDY	TRUE		2000
	EIDE_OPTICAL_INT	TRUE		2000
TRACKPAD	+5V_TPAD_SLEEP	TRUE		3000
	TPAD_F_TXD	TRUE		3000
	TPAD_F_RXD	TRUE		3000
	LID_CLOSED_L	TRUE		3000
	+3V_HALL_EFFECT	TRUE		3000
	SOFT_PWR_ON_L	TRUE		3000
	COMM_RESET_L	TRUE		4000
	COMM_SHUTDOWN	TRUE		4000
	COMM_RING_DET_L	TRUE		4000
	COMM_TXD_L	TRUE		4000
	COMM_TRXC	TRUE		4000
	COMM_GPIO_L	TRUE		4000
	COMM_DTR_L	TRUE		4000
	COMM_RTS_L	TRUE		4000
	COMM_RXD	TRUE		4000
MODEM/SERIAL	KBD_ID	TRUE		3000
	KBD_INTL	TRUE		3000
	KBD_JIS	TRUE		3000
	KBD_CAPSLOCK_LED	TRUE		3000
	KBD_NUMLOCK_LED	TRUE		3000
	KBD_FUNCTION_L	TRUE		3000
	KBD_COMMAND_L	TRUE		3000
	KBD_OPTION_L	TRUE		3000
	KBD_CONTROL_L	TRUE		3000
	KBD_SHIFT_L	TRUE		3000
	KBD_X<0...9>	TRUE		3000
	KBD_Y<0...7>	TRUE		3000
KEYBOARD	+BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000
	BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000
	BATT_CLK	TRUE		1000
	BATT_DATA	TRUE		1000
	PMU_BATT_DET_L	TRUE		1000
BATTERY	+FAN_PWR	TRUE		3000
	FAN1_TACH	TRUE		3000
	FAN2_TACH	TRUE		3000
	FAN1_GND	TRUE		3000
	FAN2_GND	TRUE		3000
FANS	MDI_P<0...3>	TRUE		1000
	MDI_M<0...3>	TRUE		1000
ETHERNET	FW_TPOGP	TRUE		1000
	FW_TPOGN	TRUE		1000
	FW_TPOOR	TRUE		1000
	FW_TPIOP	TRUE		1000
	FW_TPION	TRUE		1000
FIREWIRE	+FW_VP0	TRUE		1000
	FW_VGND	TRUE		1000

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
FIREWIRE (CONT.)	FW_TPO1P	TRUE		1000
	FW_TPO1M	TRUE		1000
	FW_TPI1P	TRUE		1000
	FW_TPI1M	TRUE		1000
	+FW_VP1	TRUE		1000
	FW_VGND	TRUE		1000
DC PWR IN	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000
LMU/ALS	ST7_SLEEP_LED_H	TRUE		23
	PMU_SLEEP_LED	TRUE		23
	PMU_LID_CLOSED_L	TRUE		23 29
	LMU_DETECT	TRUE		23
MISC.			6	1000
	SLEEP_LED	TRUE		23
	PMU_KB_RESET_L	TRUE		29
	SLEEP	TRUE		23 25 29 32 34
	PMU_CPU_HRESET_L	TRUE		6 29
	BB_RESET_L	TRUE		6
	+3V_PMU_RESET	TRUE		29 33

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SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE	SHT	OF
NONE	39	40

	8	7	6	5	4	3	2	1
	REVISION HISTORY							
	Proto Release							
	7/22/02 - Initial acquisition of schematic (from 051-6278 Rev 01) Added P59 80-DIMM connector as placeholder (p.12) Added P59 LVDS connector as placeholder (p.22) Changed J9 to 10 pin Elco connector for modem (p.25) Changed PBUS holdup caps to P59 electrolytic cans (p.30) 7/23/02 - Removed L3 (p.8) Replaced processor with 360 pin Apollo (p.5,6) 7/24/02 - Added P68 Between battery and PBUS rails for airline power (p.29) 8/10/02 - Added USB 2.0 (p.18) 8/20/02 - Removed spare pullup straps for Intrepid (p.9) Removed USB overcurrent protection [to be placed on other boards] (p.18) Changed right USB board connector to 16 pin Hirose connector (p.26) Changed L10 board connector to 40 pin Molex connector (p.26) Added 6 bypass caps to MAXBUS_SLEEP and CPU_VCORE_SLEEP (p.5) 8/26/02 - Removed 32 bypass caps for +3V MAIN at Intrepid (p.16) Removed 5 bypass caps for +2.5V MAIN at Intrepid (p.6) Removed 3 bypass caps for +1.5V AGP at Intrepid (p.16) Removed 4 bypass caps for MAXBUS_MAIN at Intrepid (p.16) 8/27/02 - Changed main battery connector to BP24067-R1, which is close to final (p.29) 8/29/02 - Added dedicated Boot Banger circuit (p.6) Added 5 bypass caps to each 80-DIMM connector (p.11) Added quad voltage circuit for bus slewing architecture (p.32) 8/30/02 - Changed to low profile 32.768kHz crystal for PMU (p.28) Changed to Q11 adapter detection scheme (p.28) 9/03/02 - Corrected upper LVDS single pin nets (p.20) Removed unintentional extra pulldown resistor at Intrepid (p.14) 9/17/02 - Numerous changes to stay in sync with P84 (all) 9/18/02 - Changed battery connector back to P84 part (p.29) Added LMU circuitry to eliminate extra board (p.23) Changed to P84 dual channel LVDS connector to reduce 12R cable losses(p.22) 9/19/02 - Removed unnecessary battery fets (due to 3S official design) (p.29) Modified chassis gnds on some components (all) Corrected LMU connector to LMU crystal (p.23) Corrected battery connector [same as P84] (p.29) Removed P93 support (p.25) Removed second fuse from FW ports [single fuse provides adequate power] (p.27) 9/23/02 - Replaced BCM5421 with Marvell 88E1111 (p.26) Increased MAX_VIA_COUNT by two on most nets with this constraint for uVia (p.34,35) 9/27/02 - Corrected cpu, memory bus constraints to match manhattan lengths (p.34) Swapped pins on L33, L35 for layout (p.31) Changed V6 to smaller foot factor crystal (p.26) 9/30/02 - Changed J19 (DC-in) to proper 4-pin connector (p.29) Corrected holes and chassis gnds (p.4,all) 10/01/02 - Removed Intrepid 1.x specific circuitry (p.13) 10/03/02 - Numerous pin-swaps to accomodate board layout (all) 10/08/02 - Added caps for functional test points (p.37) 10/09/02 - Changed 16 pin connectors (modem and right USB) to Foxconn parts (p.23) 10/10/02 - Changed NCL pins high per documentation (p.17) Added 10K pullup to CG_ADDRSEL and 10K pulldown to CG_FSEL on CY28512 (p.14) Added SSCQ/NO_SSCQ stuffing options for CY28512 circuit (p.14) Removed CPU_VCORE pullup to 5V to eliminate potential 3V/5V current path (p.32) Added Zebra 15/16 support per P84 (p.27) Added second FW port power fuse (p.27) Removed INT_CPUFB_IN cap per P84 (p.8) Replaced INT_FET2 Fets with TSPF8131n battery charger and 14V PBUS switchers (p.29,30) Renamed optical interface for consistency (p.24,37) Corrected PLL_Clock for Apollo 7 (needed to make sure be zero) (p.5,7) Removed temporary P84 constraints and finished up AGP clock changes (p.12,34) Added stuffing options to power fans off 3V or 5V (p.25) 10/11/02 - Replaced DVI EMI caps with 0201 versions (p.22) 10/14/02 - Changed J18 to RJ45 with integrated magnetics (p.26) 10/15/02 - Moved FireWire connectors and port power switch to separate page (p.28) Changed SMBus pullups to 7.15k, 1k as per 1Books/P84 [involved component net swaps] (p.29) Added 0603 resistors as shorting pads for power up and reset (p.45) Changed INT_MOD_SYNC, INT_MOD_DTI and INT_MOD_BITCLK to pulldowns per ERS [LA clk not used] (p.14) Added damping resistor option to LMU crystal (p.23) Changed INT_FST_FLEEN_PD to pulldown only [LA CLK not used] (p.13) Changed INT_FST_FLEEN_PD to pulldown only [LA CLK not used] (p.13) Removed FW_LKON from Intrepid EXTINT3 [no longer used], pullup added (p.14) Changed BNRMS_HRMS to 3V_SLEEP (p.24) Changed FW_PC_PD, FW_PC_PU resistors to 5k (p.27) Added 1K pulldown and net FW_PD2 to FW_PHY (p.27) 10/16/02 - Implemented new FW power switch and current limit (p.28) Replaced +14V PBUS to +PBUS (p.all) Added A29 adapter detection circuit (p.29) Added +PBUS current limiting circuit, removed battery charging current limit circuit (p.30) Changed FW_PHY pin 081 to make Port 1 1394a only (p.27) 10/21/02 - Updated CY28512 clock chip to Rev B (p.14) Added FW PHY pin 081 to make Port 1 1394a only (p.27) 10/22/02 - Added full support for non-zero CPU_FLL_CFG4* in run state (p.7) 10/23/02 - Changed LMU LED interface per P84 (p.23) Changed LMU JTAG/J2C pinout/pullup/pulldown strategy per P84 (p.23) Changed fan fets to S134460V per P84 (p.25) Pinned out right USB connector (p.25) Pinned out modem connector (p.25) Added 2 functional test points to wireless connector (p.24,38) Renamed FW low voltage power rails (p.27,37) P84 (p.33) Renamed Vcore VID nets to be consistent with P84 (p.33) Removed redundancy in DDR memory constraints (p.35) 10/24/02 - Changed FW DDC strap to pullup to strapping port (p.27) Cleaned up CY28512B circuit as per P84 [powered off main, output divider and strap tweaks] (p.14) Updated PCI clock series B values per P84 (p.23) Changed power rail for A10 to +5V_SLEEP (p.23) Added 0 ohm short and bypass cap for GPU VDD0V0 per P84 (p.21,37) Split FW_VEND into FW_VEND0 and FW_VEND1 (p.28,37) Added TP nets to GPU for XOR-tree testing (p.19-21) Removed fan PWM output pullups to +5V_SLEEP (p.25) Added FW thermal pad ground hole back in (p.27) 10/28/02 - Changed LMU layout (p.23) 10/30/02 - Changed fan power rails to common net (p.25) 10/31/02 - Added wireless RF_DISABLE_L pullup and AIRPORT_CLKRUN_L pulldown (p.24) 11/05/02 - Added 6 decoupling caps to CPU_VCORE_SLEEP (p.5) Broke out quad OR-gate to discrete components for better placement (p.22,29) 11/06/02 - Changed 10 uF FW current limit output cap to two 4.7 uF caps (p.28) Added 3 decoupling caps to CPU_VCORE_SLEEP (p.4) Added 9 decoupling caps to each of +5V_MAIN and +3V_MAIN (p.32) Removed C017, jumper for CPU_VCORE_SLEEP (p.35) 11/08/02 - Added decoupling cap to PMU reset OR gates (p.29) Changed FireWire PHY to Z17 (p.27) Added bulk caps to fan connectors (p.25) Added alternate chassis gnd connection for sleep LED (p.23) 11/11/02 - Removed +3V_MAIN option for P50 card (p.24) 11/13/02 - Removed LMU and associated circuitry (p.23) 11/14/02 - Implemented D3cold for all PCI devices (p.12,14,18) 11/25/02 - Renamed all components (all pages) 11/26/02 - Removed chokes from 1394a data pairs (p.27,28) EVT RELEASE							
	12/13/02 - Added 12 pF caps to source of 33MHz PCI clocks since they can not be buried (p.12) Replaced ALM1031 with AD7460 [12C Address Changes] (p.25) Added AD7460 hookups to GPU thermal diode (p.2,1,25) Added FireWire B ESD protection circuits (p.28) Removed hole from FireWire ground pad (p.7) 12/16/02 - DDR memory connector renamed to J25 (p.11) Removed J4210 from FireWire port power (p.28) 12/20/02 - Added F10,F20 as placeholders and experiment guides (p.28) Added diodes to OR +5V_SLEEP into FW_PHY power supply (p.27) 12/26/02 - Updated CPU p/ns to production p/ns (p.5) Updated PCI source clock and internal upFeading straps (p.8) Changed bootROM FWD signal to INT_RESET_L per P84 (p.9) Added C82 pulldowns per P84 (p.9) Updated Ethernet series Rs per P84 [Clocks to 10 ohms, data to 22 ohms] (p.13) Updated SSCQ/NO_SSCQ BOM option (p.14) Renamed line-in and headphone sense lines to reflect active low signals (p.14,25,39) Added 0 ohm Rs to make 2.5V Intrepid rail hot or cold (p.15,16,38) NO STUFFED entire 1.5V LDO circuit (p.15) Stuffed USB OC1/FP0N filters for 0 Ohm constant [due to new port current limiters] (p.17) Renamed USB OC1/FP0N signals for left/right ports (p.17,39) Updated GPU VCore to stay in sync with P84 [Jitter Improvement] (p.20) Added EMI caps to LVDS_DDC_CLK, INT_I2S0_SND_MCLK, INT_I2S0_SND_SCLK per P84 (p.22,25) Added R800,R801 for eventual thermal diode in CPU (p.25) Renamed R2000 to R789, R2001 to R802, R2002 to R803 (p.25) Renamed F10 to F1, F20 to F2 [deleted old F1,F2] (p.28) Added caps to FW EMI circuit that were missed (p.28) Changed MAX4172 power source to save current on battery [per P84] (p.30) Updated 1.5V/2.5V switcher BOM to stay in sync with P84 [FET change and current limits] (p.34) Replaced all 132S1061 [1uF,0805,10V,20k] with 132S0046 [1uF,0603,10V,20k] (p.14,15,27,30,33,34) Replaced all 138S0251 [1uF,0603,6.3V,10k] with 132S0046 [1uF,0603,10V,20k] (p.27,30) 01/02/03 - Updated FireWire fuse topology to that of P84 (p.28) Updated system and power block diagrams (p.2,3) 01/03/03 - Corrected +2.5V_INTREPID connections to muxes and reference (p.9,10) 01/07/03 - Added NO_TEST nets to pads of DDR connector arms (p.11) 01/08/03 - Added ZNY002 circuits to ensure speakers are muted during power-up (p.25) Changed R164 to 511 ohms to avoid low CPU clock amplitude (p.8) 01/09/03 - Added required pulldown to output of DVI_HPD sense comparator (p.22) Swapped R443 and R444 values to ensure Vgs < -4.5V (p.28) Updated S-video filter values to those of P84 (p.22) 01/10/03 - ZT7,ZT23,ZT6,ZT76,ZT89,ZT87,ZT22,ZT38,ZT60,ZT42 & ZT17 are changed to HOLE-VIA-20R10 (p.4) 01/13/03 - Add L53, L54, L55 for TMDS Data<0+2> Diff Pair (p.22) 01/14/03 - Add C821 - C821 (total 10 0.22uF caps) for 2.5V Intrepid Decoupling (p.16) Add C822 & C823 at Wireless Card connector MAIN_RESET_L & RF_DISABLE_L_SPN (p.24) Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37) Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37) Add R810 & R811 for ALWAYS-ON FANS in Acrylic Build (p.25) Remove NV31/17 components (p.19-21) 01/28/03 - Add M10 (p.19-21) 02/07/03 - Add Power Net Constraints for M10 (p.38) Replace Singing PBUS Cap C49,C50,C67,C68,C80,C81,C95,C96,C108,C109,C120,C121 with 12600035 (or alt. 1260036) (p.33) 02/11/03 - Add FW Power Net Constraints (p.38) Change signal constraints for AGP signals (p.36) Add LMU connector and components (p.23) Edit I2C table for LMU (p.13) Change R580 to 19.6k (p.14) Connect Clock Slewing RESET# to MAIN_RESET_L (p.14) Change Ferrite Bean of ATI power supply to correct values (p.21) Remove C141 PBUS CAP (p.31) 02/12/03 - Change and Rotate Keyboard Connector (p.23) Add ATI Power sequencing Circuit for M10 Power-up and Power-down (p.19-22, p.32-35)							
	EVT RELEASE (continue)							
	02/13/03 - Add C825 (p.30) 02/17/03 - Rename all Reference Designators							
	EVT ENCLOSURE RELEASE							
	03/13/03 - Change 3-P FAN connectors to 4-P (p.25) Add PU at PMU_SLEEP_LED_L for LMU (p.23) Change stuffing option for clock slewing (p.25) Change ATI M10 GPIO8 to Pull-down (p.20) Remove Memory_MUX 0ohm Resistors (p.10) 03/28/03 - Due to MLB outline change at DVI connector, CHGN01 has to be melted into CHGN1 & CHGN2 (P 4 & 22) Separate +3V and +5V traces running from 3/5V supply to 40Pin LIO connector (P 25 & 32) R601 change from 100K to 4.7K (P 29) Change airline detect to 13.1V or greater, R40 and R690 to 97.6K ohm (P 30 & 31) Add C826 at U3 RS3 - pin (P 30) Change D3 to 1N914 PN Junction Diode(P 31) 03/31/03 - Change AGPTSTEST Pull-up to 470hm (it was 400hm) (P 20) Change C643 10uF Cap to 1206 package part (P 28) Change all 1210 4.7uF to 1206 4.7uF Cap (138S0531) (various pages) Modify FAN circuit to PWM active low signal (P25) 04/08/03 - Add SOFT MODEM support (P 14 & 25) Add 10-pin ELCO connector for Serial Debug Interface (P 25) Change Q1 from S144350V to S0D45P03-10 (P 30) Remove U34 RS3AB (P 30) 04/11/03 - Change FW Schottky Diode to a 3A part 371S0159 (P 28) Change PBUS L69 and VCORE L71 inductor (P 31 & 33) Change battery fets to 3S only (p.25) Change all 6 VCORE Caps to 220uF AL Poly cap 128S0024 (p 33) Add Mitaumi MM1571J regulator to provide 1.8V TPVDD (p.2) Change U34 to Mitaumi MM1571J part for ATI FLL 1.8V rail(P 21) 04/16/03 - Add FW Port Shutdown/PowerOn Circuit (P 28) Change the I2C Pull-up for Sound/Modem to 1K ohm (P 14) 04/17/03 - Change 3V/5V inductors (152S0137) L61 & L62 (P 32) 04/21/03 - Add 12 ICT JTAG TEST PADS (P 39) 04/23/03 - Invert ATI GPIO15 signal, no stuff pull-up resistor (P 20) Combine Q35 and Q36 into a Dual Package Part (P 22) SWAP the AD7460 Temperature Sense pair (P 2) Change FW PHY to production part (P 26) 04/24/03 - Remove +3V_CBUS_SLEEP and U5, use +3V_SLEEP directly (P 14,18,24) Add 0402 Res between ATI_PVDD/TPVDD rail and 10uF caps for stability purpose (P 21) Add common mode choke at TMDS data <0,+2> pairs (p.22) Add Sense Resistor to Vcore power rail, remove one 220uF cap <back to EVTA design> (P 33) 04/25/03 - Change C826 to 0.01uF 50V Cap (P 30) 04/30/03 - No stuff R676 to prevent +3V rail leakage (P 33) 05/02/03 - L45,L46,L47 is using Common Mode Choke TDK ACM2012D Part, will replace with ACM2012H Part if available (P 22)							
	DVT RELEASE							
	05/21/03 - Swap +PBUS and +24V_PBUS at Backup Battery Connector - J16 (p.31) 05/27/03 - Change Q62 timing specification (p.13) Change Q62 & Q65 to S17860DP part (p.33) Change C843 10uF Cap to 1206 package part (P 28) Enable VCore Burst(Skip) Mode by no stuffing R67 (p.33) Enable VCore Burst Mod by changing R406 & R407 to 100K ohm (p.32) Change Q48 to IRF7832 part (p.20) Change Q49 to IRF7832 part (p.20) Enable CPUCore Burst Mode by changing R358 to 2.2 ohm, no stuffing R344 and stuffing R343 (p.20) Reduce audible noise by changing L64 to 152S0139 (p.20) Change C840,C841,C838,C844,C845 Opt caper near power switchers FETs (p.20, 32 & 34) Change PWM_L Fan Input (both L&R Fans) to +5V_SLEEP pull-up (p.25) 05/30/03 - Change C840,C838,C844,C845 Opt caper near power switchers FETs (p.20, 32 & 34) 06/03/03 - Add CPU Core Voltage offset option circuit (p.33) 06/05/03 - Change FW-B connector to S148S0058 with internal shield pins (p.28) 06/06/03 - Add four 0ohm jumper, in case there is no sw support for the multi-stage VCore (p.38) 06/12/03 - Change the +2.5V sleep FET to reduce Voltage drop on the rail (p.34) Change CBUS & USB2 REQ_LINX Pullup to +3V_MAIN (p.12) Add 0 ohm at USB AVSS_GND (p.17) Change TMDS common mode choke to TDK AMC2012-900H part (p.22) Change HD DMACLK L pullup R213 to 10K (p.24) Add C847,C851 & C852 at ENET_CLK for EMC (p.13 & 26) Change Q34 to FDS3672 (p.28) Change Q82 pin#4 connection to system digital GND (p.33) Add C848 150uF cap at J3 for +5V_MAIN USB2 power (p.25) Add C853 1000pF cap at Q64 (p.30) Add RC at AD7460 power rail for noise isolation (p.25) Isolate THERMNS signal at AD7460 by using double inverters for THERM_L_OC (p.25) Remove redundant pullup R601 for THERM_L_OC (p.29) Remove SMD EMI apings at CHGN05 (p.23) Add additional PWM/GND pins at J17 for R-USB board (p.25) 06/13/03 - New 50010M connector with 4 through-hole mounting pins (p.11) Change CPU config stuffing option at R63 and R64 (p.7) Stuff R288 for Cypress CLK chip (p.14) Move CBUS_PCI_REQ_L back to +3V_SLEEP rail pull-up (p.12) Change the TMDS Termination Resistor values to 162ohm (p.20) Connect C847 at R160.1 (p.13) Add 1000pF caps at AD7460 D+plus/minus pairs (p.25) Add S1182 DVI transmitter to prevent leakage from DVI connector to the system (p.19&20) 06/16/03 - Replace C705,C707,C711,C703 & C685 with part 128S0025 (p.20&32) Remove R271 resistor (p.34) Edit Signal Constraints for TMDS routing and ENET routing (p.36&37)							
	DVT2 RELEASE							
	07/06/03 - Change R97 & R98 to 0402 package (p.33) No Stuff R835 (p.19) Change R198 to 100K ohm resistor (p.23) Add Common Mode Choke L77 & L76 at PMB pairs (p.28) Removed current monitoring IC for firewire port power (p.28) Changed RP52,RP53,RP56,RP57 to 22ohm for EMI (p.19)							
	PRODUCTION RELEASE							
	07/28/03 - Change BOM option for C51,C52,C77,C78,C91,C92,C111 to 8.2uF Panasonic AL cap only (p. 34) 08/05/03 - Change +3V/5V ITH compensation and No-Stuff Feed Forward Caps (p. 32) Change CPU VCore setting for both BEST and BETTER configurations (p. 33) 08/07/03 - Change CPU VCore setting for both BEST and BETTER configurations again (p. 33)							
	PRODUCTION RELEASE (Version C)							
	08/18/03 - Change CPU VCore setting for BEST configuration to: 1.335V(High)->1.080V(Low) (p. 33)							
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	DRAWING NUMBER D 051-6338 C							
	SCALE NONE SHEET 40 OF 40							
	8	7	6	5	4	3	2	1